
De Vonk
Periodical of E.T.S.V. Scintilla
Year 35 | Edition 1 | February 2017
Main article: The piezo-electric field effect transistor
Internship: How to debug a complete smartphone transmitter


Scintilla
Gino Spil
I WANT YOU
TO JOIN
DE VONK

Presidential note.

Author: Guus Frijters

Hello all again, at the time of writing this presidential note, we are six months into the year. We are mostly used to the workload, and some board tasks almost feel like a habit. Of course it still happens that somethings comes on our path with which we do not directly know what we have to do with it, but there are also moments when we feel like our tasks are already finished for the day.

Something that also feels normal after these six months is the fact that I have not made and exam in almost 8 months. The last time this happened was when I broke my ankle. The time before that was when I was 6ish. This causes a few things though. It means deadlines work a little different and feedback on your work does not look anything like getting graded.

Within six months it is already visible that we are getting used to being a board and that it feels like how it is supposed to go at all times. A lot of things are even the same as it was, I still talk with a lot of members and I still visit a lot of activities. The obvious things that changed is that I am almost always in the Scintilla room.

But what does a day in the Scintilla room consist of then? A lot of the time is spend reading mail and chatting with members. Then there are a lot of meetings to attend and of course random board things. It all results in a regular work day. It almost seems that we are normal working civilians.

Luckily, to make sure we are not really employees of some company, we have a lot of possible beer moments to drink away the day and feel like a student. Either at Scintilla or at another association. As a board member you can almost drink beer somewhere everyday because you know all the right people.

So, what is it like to be a board member? After six months my experience is already quite broad. I have met loads of people from all different branches, I came in contact with a lot of people associated with the university and I even went to some companies where I represented Scintilla to show how great we, as an association, are. Not only for the students, but also for the study. So, to stay short, life as a board is good!

Op de koningin, op Scintilla

Guus Frijters

The Board is looking for you!
Are you curious in what the board of Scintilla does daily? And are you maybe interested in a board year yourself but do you have no clue as to what it is? Join us for a nice lunch to hear what it is all about on the 1st of March!

Theme Announcementdrink!
After a disciplined theme in 2016, this year's SKIC committee will announce the theme for the upcoming 2017 Kick-in camp. Intrested? Then drop by on the 13th of March in the Abscint!

96th Cantus Scintillae!
Once again, it is time for the 96th Cantus Scintillae. It is the nicest event for all members, young and old. Come and sing, drink and discuss at one of Scintillas most famous events on March 30th.

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De Vonk

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Editorial

Puzzlllleee

It is one of those nights where a lot of Vonk members gather together to make a new amazing edition of the Vonk. Some people are learning how to layout while Truusje is trying to solve puzzles in order to find the best one for this Vonk. It is quite a task, since there are a lot of puzzles online, but only the most complex are suitable for here.

Before I started writing this, I was searching for puzzles as well! I found a really strange puzzle with five stars so it was promising. Regrettable, the puzzle was a bit strange... When I wanted to take a look at the answer, it just said:" Unfortunately, we do not have our own solution available. It turns out to be an extremely complex topic." Uhm yes, how do I know the answer if they do not even know! Maybe it is something with complex numbers? Maybe they did not want to finish their last puzzle? Or is it just really that hard? We will probably never know, since Truusje chose another puzzle instead.

Now, do not turn directly to the puzzle (although I know it is the most fun thing to do during lectures), but first read some of the amazing articles we have this Vonk! After that, please do the puzzle, Truusje spent a lot of time trying to find the best of the internet.

Céline

Advertorial: Witteveen+Bos

author: dr.ir. H. Droogendijk

Within the Netherlands, there are hundreds of movable bridges located throughout the entire country. These bridges are owned be several instances, like Rijkswaterstaat, ProRail, provinces, municipalities, but also water boards. These bridges should be considered as a machine with large, moving parts and therefore they can be assessed by means of the Machinery Directive (2006/42/EG). The main goal of this directive is to establish that these machines comply with the so-called essential health and safety requirements. In other words, the movable bridges in our country need to be safe.

Risk assessment

In order to determine what 'safe' actually means, it is required by the Machinery Directive to perform a risk assessment movable bridges. By following a structured analysis the present risks are to be identified, quantified and then reduced or mitigated by taking adequate measures. A well-known method for performing risk assessment on machinery is described by ISO 12100. In the end, one will find a list of risks which need to be reduced.

Figure 1. Example of a movable bridge (Schinkelbruggen, Amsterdam).

The first step in reducing risks is to alter the design, in order that either the hazard is removed or the risk has vanished. However, in many cases this step cannot be executed due to e.g. design specifications. The second step is to look for mechanical solutions, which prevent a person from entering hazardous areas, such as physical barriers and guards. Though, there are numerous situations in which these types of solutions do not suffice. For example, if maintenance is required, one will actually need to enter hazardous areas. Then, the solution for risk reduction can be yield by functional safety.

Functional safety

Functional safety in machinery usually means systems that safely monitor and, when necessary, override the machine applications to ensure safe operation. This means that a safety-related system implements the required safety functions by detecting hazardous conditions and bringing operation to a safe state, by ensuring that a desired action, e.g. safe stopping, takes place.

Generally, safety chains are designed in order to obtain the input ('sensor'), process this input by a control system ('logic') and perform an action on the machine ('actuator').

The way safe stopping actually needs to be realized is a matter of choice and standards. The standards for electronic safety systems are formally designated by both ISO 13849- 1 for Performance Level (PL) and IEC 62061 for Safety Integrity Level (SIL).

In this article, the standard for SIL and its application on designing movable bridges is discussed, since the method of SIL is commonly used by Witteveen+Bos in projects on movable bridges.

Safety Integrity Level (SIL)

IEC 62061 is the standard for designing electrical safety systems. It includes recommendations for the design, integration and validation of safety-related electrical, electronic and programmable electronic control systems for machinery. This standard also covers the entire safety chain, e.g. sensor-logic-actuator. As long as the entire safety function fulfils the defined requirements, individual sub-systems need not be certified.

The standard defines how to determine both the required and achieved Safety Integrity Level (SIL). SIL represents the reliability of safety functions. Four SIL levels are possible: 1, 2, 3, and 4. 'SIL 4' is the highest level of safety integrity and 'SIL 1' the lowest. In the field of machinery (and thus movable bridges), only levels 1-3 are used.

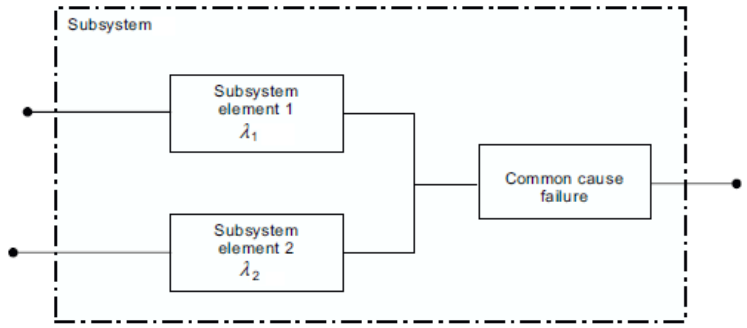


Figure 2. Example of a subsystem for a safety chain

Dangerous failure

In IEC 62061, a safety integrity requirement is expressed as a target failure value for the probability of dangerous failure per hour, PFH_D, as shown in table 1. A dangerous failure is to be considered as a situation where a malfunction of the system will lead to a dangerous situation (like unexpected movements of the machine).

Additionally, there exist threshold values (per hour) for systems that do not contain sufficient diagnostic coverage (e.g. automatic diagnostic tests on proper component operation). This coverage DC can be expressed as the ratio between detected dangerous hardware

$$DC = \frac{\Sigma\lambda_{DD}}{\Sigma\lambda_{D,total}}$$

failures, $\sum\lambda_{DD}$, and the total of dangerous hardware failures $\sum\lambda_{D,total}$:

Determination of the value of PFH_D depends of the design of the safety chain and choice of components and can be quite complicated. An example is given below, where a system is considered with single fault tolerance (i.e. redundant architecture) and without a diagnostic function. Note the presence of the common cause failure (CCF), for which a single fault will lead to a failure by both channels.

Safety integrity level	Probability of a dangerous Failure per Hour (PFH_D)
3	$\geq 10^{-8}$ to $< 10^{-7}$
2	$\geq 10^{-7}$ to $< 10^{-6}$
1	$\geq 10^{-6}$ to $< 10^{-5}$

Table 1. Overview of safety integrity levels

For such an architecture, the probability of dangerous failure of the subsystem is:

$$PFH_D = \lambda \times 1h,$$
$$\lambda = (1-\beta^2)\lambda_1\lambda_2 T_1 + \beta/2\,(\lambda_1+\lambda_2)$$

where T_1 is the proof test interval or lifetime (smallest), β is the susceptibility to common cause failures and λ is the failure rate.

Architectural constraints

To realize a system which yields a sufficient integrity on safety, there are generally two approaches. The first approach is to consider hardware fault tolerance, by designing a system using a redundant architecture (e.g. the previously mentioned subsystem). Though, there are limits on what can be achieved on SIL, by considering table 2, due to the lack of diagnosis.

Diagnosis

As can be derived from the analysis on architectural constraints, the other approach for achieving safety integrity is to design a 'smart' system. Such a system contains several diagnostic functions in which dangerous failures are either early detected or will lead directly lead to a

Safe failure fraction	Hardware fault tolerance (see Note 1)		
	0	1	2
< 60 %	Not allowed	SIL1	SIL2
60 % – < 90 %	SIL1	SIL2	SIL3
90 % – < 99 %	SIL2	SIL3	SIL3 (see Note 2)
≥ 99 %	SIL3	SIL3 (see Note 2)	SIL3 (see Note 2)

NOTE 1 A hardware fault tolerance of *N* means that *N*+1 faults could cause a loss of the safety-related control function.

NOTE 2 A SIL 4 claim limit is not considered in this standard. For SIL 4 see IEC 61508-1.

Table 2. Architectural constraints for SIL

safe condition of the system.

From this table, the so-called safe failure fraction SFF determines which SIL can be achieved by implementing a specifically chosen hardware fault tolerance. The expression for SFF is:
where $\sum\lambda_S$ is the rate of safe failure (when a fault leads to a safe state/ stop), $\sum\lambda_{DD}$ is the rate of dangerous failure which is detected by the diagnostic functions and $\sum \lambda_D$ is the rate of dangerous failure.

$$SFF = \frac{\Sigma\lambda_S + \Sigma\lambda_{DD}}{\Sigma\lambda_S + \Sigma\lambda_D}$$

Safety chain example

To illustrate how such a safety chain can look in practice, consider the example below. Here, two emergency stop buttons in series are considered, that are connected to a safety-PLC (i.e. redundant processors, I/O, communications etc.). From this PLC, two actuators (contactors) in series are controlled, that can switch the main current to the driving motor. Diagnostics are implemented by proper configuration of the safety PLC: the input is monitored by e.g. cross-monitoring contacts of the emergency buttons, whereas the output is monitored by exploiting feedback on the contactors. By using a redundant architecture (hardware fault tolerance equal to one), safety components and diagnostics, this safety chain is suitable up to SIL3.

Conclusion

Safety for movable bridges can be achieved in several ways. Today, the majority of risks for these type of bridges are reduced or mitigated by means of functional safety, wherein a safety chain will bring the bridge control system in a safe state (e.g. stop). Key aspects of designing these safety chains are failure rate, choice in architectural constraints and diagnosis.

Further reading

See standard IEC 62061.

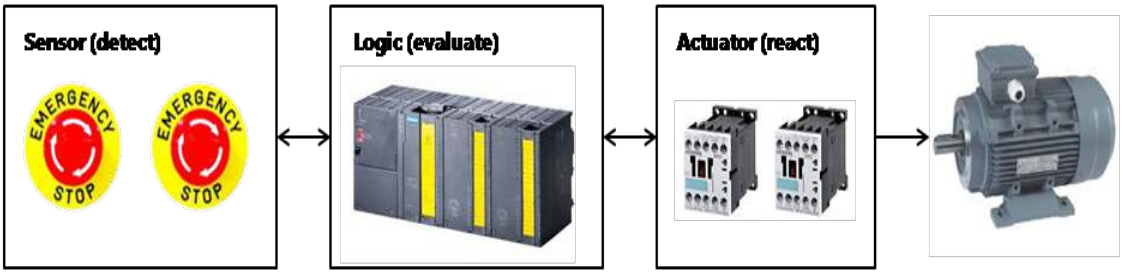


Figure 3. Example of a safety chain with redundant architecture and diagnostics.

Module 7

Authors: Nahuel Manterola.
Mark van Holland

Within a few weeks, second year students will have to make a choice for the seventh module: Network Systems or Device Physics. This article will hopefully shed some light on both modules, and aid you in your choice.

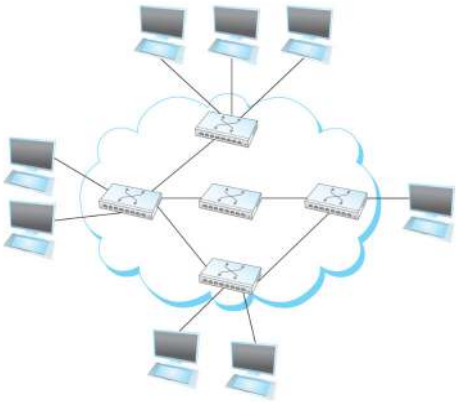
Network Systems:

This module treats communications between different systems. If you're interested in how the internet works, which protocols are used to communicate and how data is encrypted, this might be the right module for you.

The schedule of network systems is quite stable. Every week there are two lectures, two tutorials, an observation lab and a challenge. While the lecture and tutorials are quite straightforward, the lab and challenge are less so. In the observation lab, you will use Wireshark, a program which can track and display all packets sent to and from your computer. In the weekly challenge, you will have to program a part of a communication system in groups of two. On a central screen the scores of each team will be displayed live, which creates a fun competition. One minor problem with the challenges was the understaffing. The three available teaching assistants had to rush from one table to the other to help people, and only one of them knew how to program in C++. This might have been fixed this year, though. The day of the challenge will also be the only day in the week you need to work hard, because the module in general gives you a lot of 'self-study'. For the challenge and final project, you will learn to program in C++. This will be one lecture and one tutorial in a week, in which you will learn how to program quite in depth. Several types of sorting, recursive functions and multi-threading will be treated. The other lecture and tutorial will be the main course on network systems, mostly taught by Pieter-Tjerk de Boer, a very energetic and passionate teacher who really loves the subject. For the biggest part, the lectures are easy to follow. Every three weeks there will be a test. The tests of last year were open book, and were very easy to pass. Keep in mind that this means you need to buy the book, since you will need it at the tests.

The project at the end of the module covered almost two full weeks. It combined just about everything you've learned in the module in a single assignment: making an ad-hoc network, in which users can chat with each other. The messages needed to be encrypted, and should also be routed through another computer if the goal was not within the senders reach.

This module will be a relief from module 6, since it doesn't require any important calculations like you're used to from other modules. Even though the module isn't very hard, you'll learn quite a lot.
To round it up, Network Systems is a module with low workload, in which you will learn a lot about network systems like the internet, and will also learn to program in C++.



Device Physics

Device physics is one of the modules that can be chosen in module seven. Device physics focuses on the workings of nanoscale devices like transistors and LEDs. The module consists of PBLs just like in module four. As the project for this module, you will get one of the following options, making a photodiode, making a MEMS device or doing the Haynes-Shockley experiment.

For the module you get split up in groups of about 4 people, to work on the PBLs and the project with. For each PBL you have 2 days the time to make them. Before we went to work for ourselves we got a little introduction lecture, to introduce the subject to us. Here the basics of the theory we were going to work with and at the end the problem was introduced to us. For my group and a lot of the other groups this just meant that we worked longer than planned on the PBL for the first day, so that we could sleep in the other day and gather around ten o'clock.

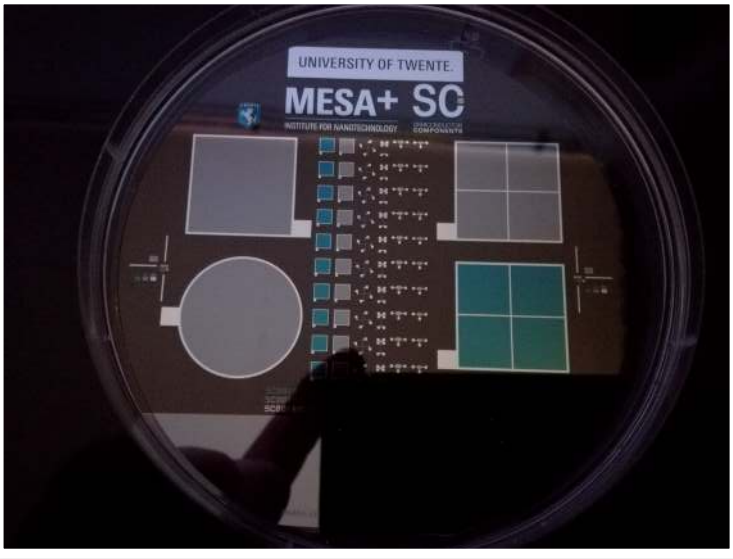
On the second day of the PBLs we needed to present our solutions to the problem, you would think this would mean hearing the same story like four times in a row, but usually it was the case that the different groups had some different solutions to the different problems and for the problems they could not solve another group usually had an answer. After we all presented our solution, the teacher would tell us his solution and if we missed anything explained something a bit more. The subject touched on in the PBLs were about quantum mechanics, photonics, semiconductor devices, and semiconductors.

> "We worked longer than planned on the PBL for the first day, so that we could sleep in the other day and gather around ten o'clock."

My group got assigned to the photodiode project. For this project we needed to design a photodiode (what a surprise!). In the beginning we needed to find out how a photodiode worked, so we knew what we were designing and how we could make better photodiodes. In the project we looked at the effects of the form and size of the photodiode. When we were done designing the photodiode, we went to the Nanolab to make our photodiode ourselves. It was very nice to do and to see how everything was done there. When we went to the Nanolab we needed to wear these suits that made sure that you did not compromise the clean nature of the cleanrooms in the Nanolab. After making the photodiode we got to test the devices we made ourselves and got to see the different effects we were looking for and also to see who did a better job in the lab.

The other project options were the MEMS project and the Haynes-Shockley project. The goal of the MEMS project was to create nanoscale devices. The device you wanted to make was of your own choosing, as long as it followed a certain set of rules. The device you designed here was than made for you and you could choose to do measurements on it, this was however optional. For the Haynes-Shockley experiment, you were required to do the Haynes-Shockley experiment.

The test of all the subjects were at end of the module, here you get four tests for the four different subjects. The re-exams were a week and a half later.



The piezo-electric field effect transistor

Author: Raymond J.E
Hueting and Jurriaan Schmitz

The size of transistors in digital logic is ever decreasing. One of the undesired side effects of this size reduction is an increase in the leakage current with every new generation. This results in unnecessary power consumption in modern logic circuits, like microprocessors. In a normal transistor, in which the switching principle is based on electrostatics, the leakage current is determined by diffusion and therefore theoretically limited. By combining electrostatic with electromechanical switching this limit can also be broken. The semiconductor components group (SC) has recently shown this both theoretically and confirmed this experimentally by encapsulating a field effect transistor with a piezo-electric film.

Miniaturization

Until the early nineties of the previous century the development of microchips was fairly straightforward. Improved manufacturing techniques especially the ability to make increasingly small transistors in a very reproducible way lead to microchips with improved performance at reducing cost. Proper downscaling of transistors (in particular field-effect-transistors) led to a reduction in size and hence manufacturing cost while simultaneously reducing power consumption and increasing switching speed. This was a scenario with only winners. The only drawback was that the increased number of transistors in each new generation of chips led to an increase in power dissipation and the need for stacks of cooling blocks to keep the operating temperature of the processors more or less under control.

The rapid development of portable electronics warranted a different optimization of microchips in which the power consumption became the most crucial factor. This is an area that still has lots of room for improvement. According to the Landauer principle, the minimum amount of energy needed to flip a bit in an information system is only kT ln(2), where k is Boltzmann's constant and T the absolute temperature [1]. At room temperature this is only the fringy amount of 2,87 x 10^{-21} Joule! Present day electronic systems surpass this by several orders of magnitude, although each generation of chips does become more energy efficient than its predecessor.

In a microprocessor a significant amount of energy is consumed by charging and discharging parasitic capacitors, something that happens every clock cycle. On top of that there are leakage currents from the supply to the ground. In the last decade, a significant effort had been made to reduce these parasitic losses, mainly by reduction of the supply voltage.

The leakage current in a transistor

To understand this we have to study the field-effect-transistor as a non-ideal switch. Figure 1 shows this switch where the gate bias tunes the resistance between the source and drain leading to a nonlinear relation between the current and the voltage. An ideal switch would have infinite current above the turn-on voltage and no current below this threshold. Real life transistors have a limited on-current due to internal resistance and a non-zero off-current (leakage current) since some electrons can diffuse from source to drain even when the gate bias makes this difficult.

To study this leakage current in more detail it is plotted on a semi-logarithmic scale as in figure 2. When we want to reduce the supply voltage in order to reduce the active power we have to reduce the threshold voltage, shifting the entire curve to the left. This immediately results in a significant increase in the off-state current. Since the nineties the leakage has increased by 4 orders of magnitude and a further increase is no longer acceptable. The only way out of this catch-22 situation is an increase of the slope of the current-voltage curve from "off" to "on".

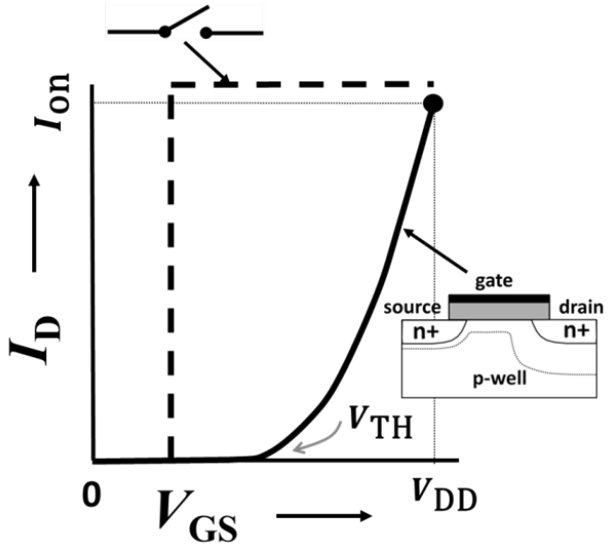


Figure 1: Schematic drawing of the current-voltage curve of a field effect transistor (solid line) and an deal switch (dotted line). The threshold voltage (VTH) is also indicated.

This is where the cookie crumbles. The leakage current between source and drain in a field-effect-transistor is caused by diffusion. When the gate potential forms a barrier, the electrons can only transfers by thermal diffusion limiting the slope in figure 2 to a maximum of 60 millivolt per decade (at room temperature). This means that for every 60 mV increase in the gate-bias the source drain current increase by one order of magnitude. In practical chips most transistors of the smallest generations do not achieve this value and a slope of 80-90 mV/decade was considered normal for a long time. In 2011 Intel introduced the TriGate transistor, that approaches the 60 mV/decade limit [2].

To take the next step the temperature needs to be reduced significantly in order to suppress the diffusion current. This has successfully been applied in supercomputers but is not feasible for portable electronic applications. This means a radical change in the transistor itself is needed to break this diffusion limit (often referred to as the "Boltzmann tyranny"). The number of scientific articles about efforts in the field of so-called steep slope transistors has skyrocketed the last decade. Several groups have demonstrated that it is possible to achieve a slope steeper than the diffusion limit of 60 mV/decade at room temperature with devices based on tunnel currents or avalanche currents, but none of these alternatives has been introduced into mass production. It is also possible to make an electro- mechanical switch (like a relay) to achieve very steep switching behavior.

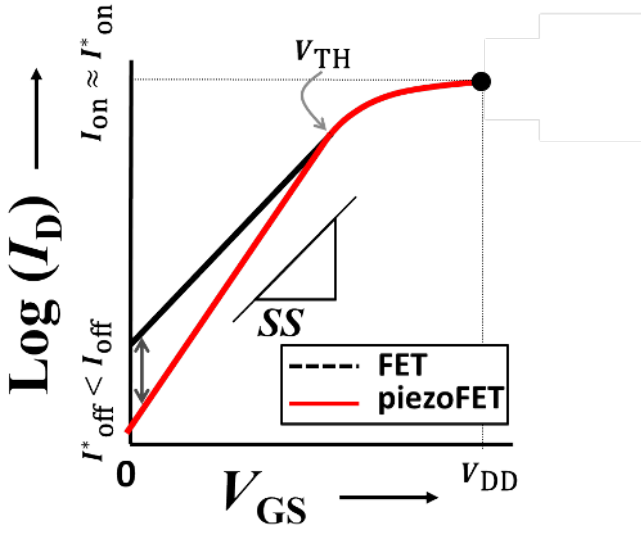


Figure 2: Schematic drawing of the current-voltage curve on a semi-log scale of a classical transistor (compare to Figuer 1) and the piezoFET ("p-FET"). The slope of the graph, the subtreshold swing (SS) is also.

The piezoFET

The group Semiconductor Components has studied such an electro-mechanical transistor. The proposed transistor utilizes the fact that the properties of a semiconductor crystal change under elastic (reversible) deformation. Recent generations of computer chips on the market make use of silicon that is severely mechanically stressed. By optimizing the direction of the mechanical force with respect to the crystal orientation, the mobility of the charge carriers (electrons and holes) increases, resulting in improved switching speed of the transistors [3],[4]. The dimensional change (strain) is expressed as a percentage (expansion or compression of the lattice), and is in the order of 1%. This means an increase of both the on- as well as off-current for realistic transistors.

These existing devices make use of permanent deformation. The novel piezoFET the SC group has developed utilizes variable mechanical deformation (tunable strain) achieved through the reverse piezo-electric effect [5]. Using this effect we have no strain in the off-state of the transistor combined with a high strain value (1-2%) in the on-state.

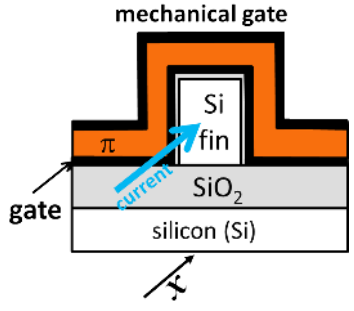


Figure 3: (a) schematic cross section of the piezoFET perpendicular tot he current direction.

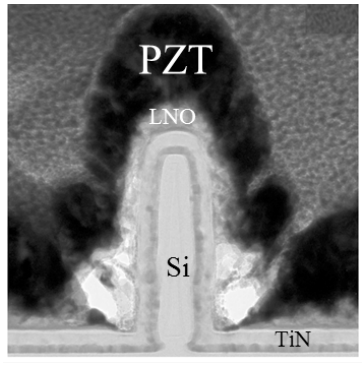


Figure 3: (b) micrograph of the cross section taken with an electron microscope.

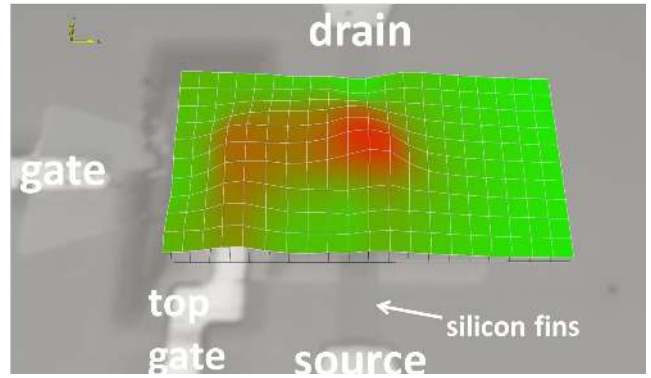


Figure 4: Topview of the upward motion of a piezoFET with 5 parallel silicon fins resulting from the piezo-electric actuation, as measured by laser doppler vibrometry. The green areas do not move, the red ones do move when a bias of 1V is applied to the piezo-electric material.

This increases the current-slope and at the same time we keep the leakage current low (see figure 2).

Figure 3(a) shows a schematic cross section of a piezoFET (piezo-electric field-effect transistor) where the transistor is encapsulated by a layer of piezo-electric material that is connected to the gate. In this way the gate not only has an electrostatic but also an electromechanical influence on the silicon. In other words, during turn-on of the piezoFET the conductive properties are enhanced due to the positive feedback of the mechanical coupling on top of the electrostatic effects.

The shape of this piezoFET deviates from conventional transistors in order to meet mechanical and electrical boundary conditions: it is a nanowire with high aspect ratio. This configuration is also called "finFET" [3], since the shape resembles a dorsal fin of an imaginary shark swimming in the silicon.

Figure 3(b) shows a transmission electron microscope cross section of a prototype piezoFET realized in the nanolab of the MESA+ institute [5]. The piezo-electric material is lead-zirconium-titanate (PZT) deposited by the company SolMateS B.V., Enschede. PZT is a very attractive material thanks to its relatively large piezo-electric constant, meaning that a relatively low electric field generates significant amounts of strain. Proof that the piezoFET really works can be found in the mechanical action. Figure 4 shows a measurement with a laser doppler vibrometer. When a bias is applied to the PZT layer an upward displacement of approximately 100 picometer in observed.

Figure 5 shows the measured current-voltage curves of a finFET with and without a PZT layer. We clearly observe that the transistor with the PZT layer (the piezoFET) has a steeper slope, of about 75 mV/dec, meaning a factor 5 reduction in the leakage current. When the PZT layer is biased with a fixed potential with respect to the gate potential the slope can be improved to 68 mV/dec (see inset). To verify the result the electron mobility was characterized. These measurements show an increase of 20-50% in the mobility with increasing strain levels.

The future

The initial experimental results are very promising and motivates to further optimize the piezoFET. First of all a relatively large distortion is observed in the laser doppler vibrometer measurements, indicating that a significant portion of the deformation is directed outward instead of inward towards the silicon. The silicon only experiences the maximum amount of stress when the surroundings do not allow free movements. We plan to improve this by encapsulating the piezoFET with a stiffer material. Additionally a reduction in the distance between the piezo-electric layer and the silicon channel can help to reduce mechanical losses. Finally replacing silicon by a less stiff semiconductor with a high deformation potential could increase the desired effects. Examples are germanium (Ge) and III-V semiconductors like indium-arsenide (InAs) or indium-antimony (InSb). An additional benefit would be the higher carrier mobility in these materials in comparison with silicon. Computer simulations of such a piezoFET structure suggest a slope as steep as 50 mV/dec at room temperature should be feasible [7], giving a factor 30 in reduction of leakage current.

Alternative transport mechanisms like tunneling can also be considered to replace conventional diffusion transport yielding an extra reduction in slope according to our calculations.

To improve the energy-efficiency of microchips the reduction of the leakage current beyond the diffusion limit would mean an important breakthrough. Electrical Engineers would need to implement physical principles previously unused like the mentioned electro-mechanical transduction and quantum-mechanical tunneling currents. In a few years the transistors may look completely different from what we have all learned from textbooks.

Intermezzo

As illustrated by figure 2 the current in a transistor operated below the threshold voltage has an exponential relationship with the applied gate-source bias (V_{GS}) [8]:

$$I_D = I_{OFF} \cdot \exp\left(\frac{V_{GS}}{m \cdot u_T}\right) \cdot \left(1 - \exp\left(-\frac{V_{DS}}{u_T}\right)\right) \quad (1)$$

where u_T is the thermal voltage, V_{DS} is the drain-source voltage, m is the ideality factor and I_{OFF} is the off-state-current. This curve is also called the "sub-threshold" curve and is caused by the diffusion transport mechanism of electrons. In the subthreshold domain electrons experience a relatively large potential barrier in the silicon under the gate, caused by the forbidden band ("band gap") of the silicon and the p-type substrate containing a relatively large amount of holes. In this situation the electrons are the minority charge carriers in the silicon under the gate. Similar to an ink spot diffusing in water, the electrons can diffuse due to thermal motion in the direction of reducing concentration; i.e. the direction of the drain, as given in the right-hand term of equation (1).

The potential barrier is lowered by increasing V_{GS} . According to the exponential relationship between potential energy and electron concentration, the current will increase exponentially with increasing V_{GS}, as described in (1).

As shown in figure 2 to reduce the leakage current we need to obtain a steeper slope in the subthreshold regime. This slope is characterized by the subthreshold swing [8]:

$$SS \stackrel{\text{def}}{=} \frac{dV_{GS}}{d\log(I_D)} = m \cdot u_T \cdot \ln(10) \quad (2)$$

In the ideal case , at room temperature, the SS≈60 mV/dec (m=1), in other words each 60 mV increase in voltage results in a tenfold increase in current. The parameter m depends on several physical parameters such as depletion charge and recombination centres at the interface between Si/oxide caused by non-idealities called traps. These parameters make m larger than 1 making the subthreshold slope larger than the ideal minimum of 60 mV/dec. This becomes an increasing problem at smaller generations of transistors. Our idea is to decrease m, to reduce the leakage current.

In case of the piezoFET the following relation can be deduced:

$$m = \frac{C_{ox} + C_{it}}{C_{ox} \cdot \left(1 + \frac{d\chi}{dV_{GS}}\right) - \frac{C_{it}}{2q} \cdot \frac{dE_g}{dV_{GS}}} \quad (3)$$

with C_{ox} the oxide capacitance per unit gate area, C_{it} is the interface trap induced capacitance per unit gate area, q is the elementary charge, χ is the electron affinity and E_g is the band gap of the silicon. C_{it} is a measure for the amount of traps at the Si surface capable of capturing charge carriers. By drastic reduction of C_{it} and an increase of the strain component $d\chi/(dV_{GS})$ it is possible to reduce m to a value below 1, making the SS lower than 60 mV/dec (see equation (2)). The piezoFET is a device that makes this possible.

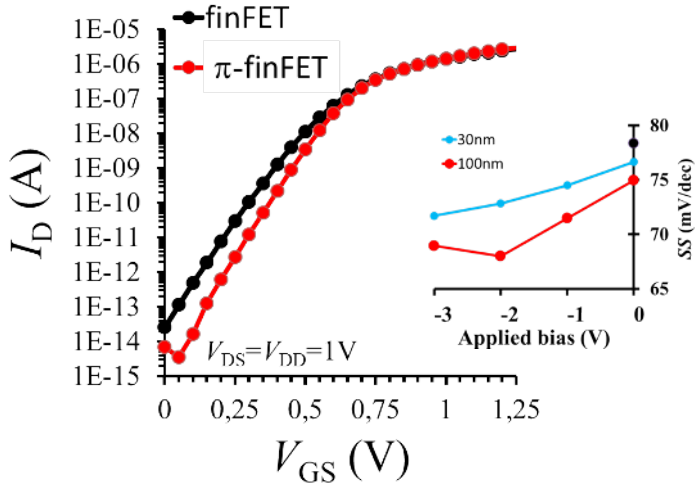


Figure 5: Current-voltage curve of the piezoFET and the regular finFET (fin-width 100 nm). The inset shows the influence of the permanent bias over the piezo-electric material on the SS for two widths: 30 and 100 nm. The measurements are done at room temperature.

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Translation by Cora Salm

Bachelor assignment

The Radio Frequency Interference Environment Behind the Moon between 0.3 -30 MHz

Author: Gerolf Meulman

For my bachelor assignment, I did a research at the Telecommunication Engineering group. As the title of my research suggest, it is about radio frequency interference at low frequencies at the other side of the Moon. Because it is very difficult to go there and do some measurements myself, I mainly looked at other literature. Nevertheless, I was able to draw some interesting conclusions.

In the study of several processes in the universe, observations at low frequencies (0.3 MHz – 30 MHz) will give valuable information. These observations cannot be done on the Earth's surface due to the obstruction and scintillation by the Earth's atmosphere at low frequencies. Therefore observations have to be done in space. The Orbiting Low Frequency Array (OLFAR) project for example aims to develop a radio telescope consisting of multiple satellites to conduct these observations. To protect observing satellites in space from radio interference from Earth, the Moon might be used as a shield. It is however not known how well the Moon can function as a shield, and therefore I have examined several sources of interference and propagation mechanisms.

The RFI produced by the Earth has three main sources. The power and the frequency range of these sources are important for the determination of the amount of RFI that will be observed behind the Moon. Another important aspect which has to be accounted for is the location where the RFI is produced. RFI produced high above the atmosphere results in a much smaller cone of RFI shielding behind the Moon than if the RFI is produced at the Earth's surface. The three sources that I have examined are artificial radio transmissions, lightning discharges and Auroral Kilometric Radiation (AKR), which I will discuss shortly here.

Artificial radio transmissions

An important source of RFI is artificial radio transmission. These transmissions are used for mobile radio communication, broadcasting, radar, navigation systems, communication satellites and many more applications. The frequency range of interest, 0.3 to 30MHz, is especially used for AM radio broadcasting, maritime mobile and (maritime) radio navigation [ ].

Artificial radio transmissions are produced on the Earth's surface. To reach the Moon, these signals first have to propagate through the ionosphere. This will attenuate these signals a lot at especially the lower frequencies. Radio transmissions below 3 MHz are effectively blocked by the ionosphere, therefore only artificial radio transmissions above 3 MHz will be accounted for. The strength of the interference above 3 MHz at Moon distance can be up to 30 dB above Galactic Background Radio Noise, which is the signal we are interested in.

Lighting

Another main source of RFI that I looked into is lightning. On the entire Earth, there are approximately 40 to 50 lightning discharges per second. Every lightning discharge generates an electromagnetic wave so powerful that it can be detected more than 10.000 km away [ ]. Therefore it might also be strong enough to be observed in space.

The RFI generated by lightning originates close to the Earth's surface, and therefore it has to propagate through the ionosphere too. It appears that the frequency of the RFI produced by lightning is especially between 0.1 and 10 kHz, which will therefore be blocked by the ionosphere. The RFI produced by lightning that does appear in above 3 MHz is approximately of the same strength as the artificial produced radio waves (+30dB).

AKR

The third main source I looked into is Auroral Kilometric Radiation (AKR). AKR radiates at the frequency band of 100 kHz to 600 kHz. This is only a small part of the frequency band of interest, but due to its high power it might saturate the receivers and is therefore very important. The AKR is the result of interaction between solar winds and the Earth's magnetosphere. This interaction takes place at an altitude of two times the radius of the Earth (RE) above the Earth's surface, which is above the ionosphere. This means that the ionosphere only attenuates the radiation directed to the Earth's surface. The AKR directed towards the Moon does not travel through the Earth's ionosphere and is therefore not attenuated by it. The high altitude of approximately 2 RE also decreases the size of the cone behind the Moon where there is no direct line of sight to the source. The strength of the AKR interference at Moon distance can be up to 70 dB above the Galactic Background Radio Noise. The frequency range of the AKR is usually between 100 – 600 kHz, but will sometimes peak up to 1MHz.

One of the main sources of my research is data collected by the RAE-B explorer from NASA. This satellite was placed into lunar orbit on 15 June 1973, to do measurements in the 25 kHz – 13.1 MHz range. A graph of the intensity of the RFI observed by the RAE-B satellite can be found in figure 1. The upper graph displays the dynamic spectrum of the observed intensities over time. The other plots display intensity vs. time at a single frequency. From immersion to emersion the Moon was in between the satellite and the Earth. In the upper plot of the figure, the AKR can be seen very clearly as a dark band between 0.18 MHz and 0.60 MHz.

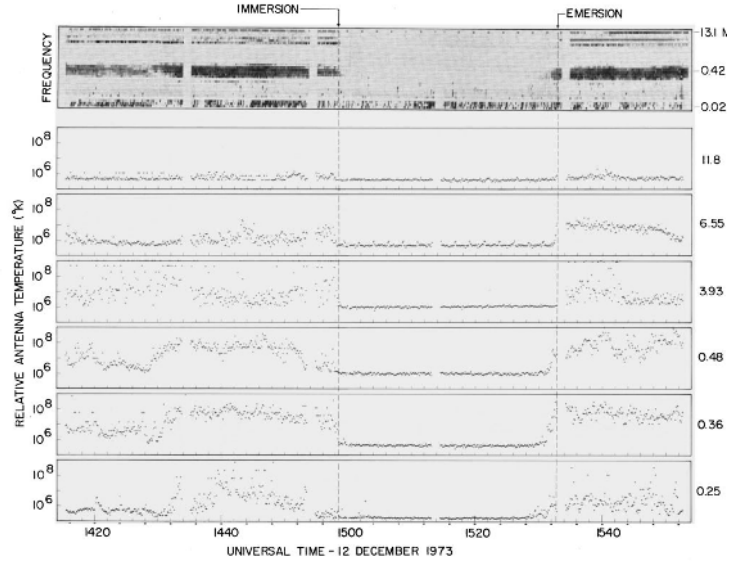


Figure 1: Relative antenna temperature observed by the RAE-B Explorer [iii]

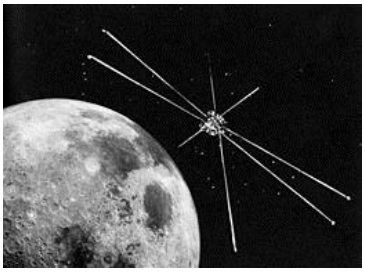
AKR is produced at an altitude of 1 – 3 times the radius of the Earth. At the beginning and the end of an occultation by the Moon, the source of AKR at this higher altitude will still be in line of sight while the Earth itself is not visible. Therefore, the RFI due to AKR will be observable for a longer period of time than RFI produced at the surface of the Earth. This is also visible in the data of the RAE-B explorer. In the figure, the interference levels at various frequencies during the occultation are shown. At 0.25, 0.36 and 0.48 MHz, and also in the upper plot, it can be seen that before the end of the occultation there is already RFI observed at these frequencies. This is the RFI due to the AKR. The interference produced at the Earth's surface, for example at 3.93 MHz, cannot be observed until the occultation is over. The "straight line" of signal that can be observed during occultations is the Galactic Background Radio Noise, which contains the interesting signals that we are interested in.

Under some conditions, which are estimated to occur around 10% of the time, the AKR is refracted at an altitude of 20-40 RE [ ]. When this happens, the altitude of the LOS-free zone above the Moon's surface will be at most 1700 km. Satellites in orbit at an altitude higher than 1000 km will be in the LOS of the interference almost all the time. This also happened to the RAE-B Explorer, which was in orbit at an altitude of 1100 km above the Moon's surface. During the refractions, the satellite was in LOS during the entire occultation as shown

in Figure 2. In this data of the RAE-B Explorer it can be seen that interference from other sources above 1 MHz is effectively blocked by the Moon during occultations, while the AKR interference at the lower frequencies is almost unaffected.
When this happens, the interference at observing satellites will likely be too high to conduct observations, and saturation of the measurement equipment may occur. Therefore, data collected under these conditions will probably have to be discarded.

Conclusion

From the information I collected about the different sources and propagation mechanisms it can be concluded that the Moon can act as a shield against RFI produced by the Earth.
Interference produced at the surface of the Earth, artificial radio transmissions and lighting, are effectively blocked by the Moon. Below 3 MHz, these signals are already attenuated a lot by the ionosphere of the Earth, and above 3 MHz the attenuation due to other propagation mechanisms (not discussed here) is so high that the surface produced RFI won't be observed behind the Moon.
The Auroral Kilometric Radiation (AKR) is more troublesome because it is not produced at the surface, but at an altitude of 1-3 times the radius of the Earth. This means that it does not have to propagate through the ionosphere to reach the Moon. The AKR has a frequency range of 100 kHz – 1MHz. These low frequencies are less attenuated by ground wave propagation. However, due to the very low conductivity of the Moon's surface and the very rough terrain, the RFI produced by AKR will still be much weaker than the Galactic Background Radio Noise when there is no direct LOS.
However, due to the high altitude of the AKR, there will be a smaller area behind the Moon where there is no direct line of sight (LOS) to the source, which reduces the amount of time where observations can be executed during a Moon orbit. For a satellite at the Earth-Moon 2nd LaGrange point, it is even worse. This point is located outside the LOS-free area, and therefore satellites located there will be directly exposed to RFI produced by the AKR. Because the interference will be very significant, this



location is not suitable for projects like OLFAR.
Another problem is the reflection of the AKR at an altitude of 20-40 times the radius of the Earth. During these reflections, RFI produced by AKR will directly travel to the backside of the Moon and satellites will not be able to do observations in orbits higher than approximately 1000 km. Fortunately, this occurs only approximately 10% of the time. Therefore, 90% of the time, observations will still be possible and the Moon will act as a shield.

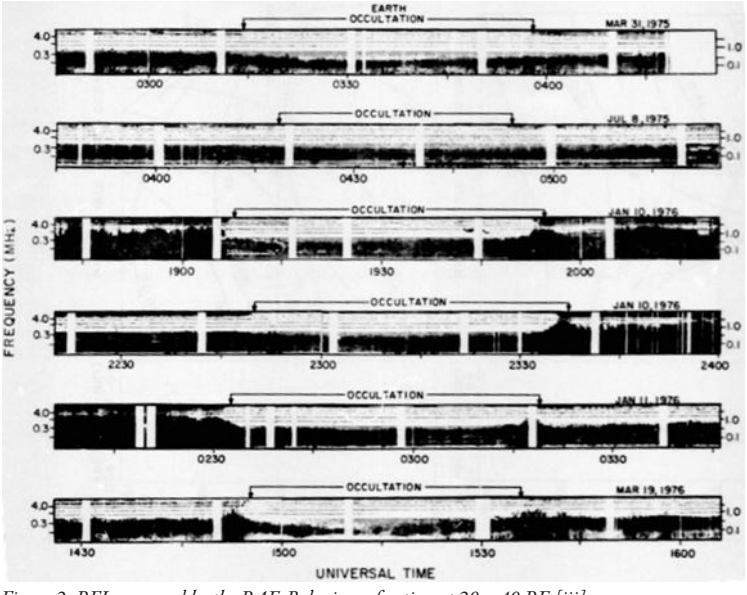


Figure 2: RFI measured by the RAE-B during refraction at 20 – 40 RE [iii]

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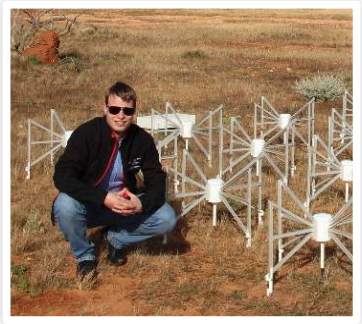
Master Telecommunication Engineering

Author: Robert Grootjans

Once upon a time in a student life there comes a point at which he/she has to decide whether to do a Master or not. For most of us it is a given to continue to the master to specialize in a certain field. So what to choose? One of the great things about electrical engineering is that almost everything in the world requires electronics, everything from robotics to biomedical systems. Since the second year I had a passion for antennas and high frequencies, so I chose to specialize in telecommunication engineering. In this article I wish to highlight my path from bachelor student to freshly graduated engineer.



Courses

First up when beginning with your master is choosing a suitable track of courses. I already knew I wanted to graduate at the research group of Telecommunication Engineering (TE). I choose a combination of integrated circuit design courses in combination with TE courses. This meant that I learned everything from transistor design to receiver architectures to radio wave propagation models. Other things that I learned were microwave structures, antennas and information theory. In total I obtained a complete package as a Radio Frequency (RF) engineer. Some courses I highly recommend choosing: Microwave Techniques, Mobile Radio, Smart Antennas & Propagation, Advanced Analog IC Electronics and Wireless Transceiver Electronics. After completing your courses you have to do a mandatory Industrial Training (internship).

Internship

One of the nice parts of doing a master is doing an internship abroad, luckily I was fortunate enough to have a fantastic opportunity to go to the International Center for Radio Astronomy and Research (ICRAR) in Perth, Western Australia. I was tasked with fully characterizing a true time delay analogue beamformer used for the Square Kilometer Array (SKA). The SKA is an international project to develop the world's largest telescope for low frequencies (the largest operational telescope at the moment is LOFAR based in the north of the Netherlands). The beamformer I had to characterize was a prototype with poor software and an undocumented interface. The 32 channels were controlled by a computer program which had 10 check buttons per channel. The delay of every channel was 8 bits. To fully characterize the beamformer it was necessary to go set every delay possible and gain settings for every channel. This meant that I needed software to automate it, or to click a whole lot of buttons for every measurement.

Figure 1: The beginning of the Square Kilometer Array in Western Australia

So after arriving, the first thing to do was to decide with a colleague on a more viable solution, than trying to obtain source code from the company that made the prototype beamformer. The reason we opted for reverse engineering was that due to politics the company was in no hurry to supply us with software. After inspecting the MODEMs used to control the beamformer it was no surprise to see that the interface used was a standard usb to rs232 chip (FT232), after two days of sniffing data and guessing baud rates we were able to divide the data into packets. As soon as we had done this we had to recreate a startup sequence and set a port via Matlab, after this succeeded we had enough to automate the beamformer without actually knowing what we were doing (copying packets does not equal understanding the protocol).

With the ability to automate the beamformer using matlab, all the measurements could be done to characterise the beamformer. With my script all the parameters could be measured with relative ease. So hooking up a vector network analyzer to every individual channel and running the script took about 20 minutes. With 32 channels this meant a great deal of measuring time where I would be drinking coffee waiting for matlab to send me an email to inform me that the measurement was completed. After all the measurements were completed by matlab it took me a good two weeks to create a report of the characterization and analyse the incredible amount of data produced. The typical measurements that were done were: gain, phase delay, compression point, non linearities and noise figure. An interesting scenario occurred when we were doing noise figure measurement. The connectors we used (QMA) were prone to leakage of RF radiation, so disturbances leaked in and showed up on the measurements when the connectors were put under mechanical stress. Another interesting learning moment is that it is wise to connect every USB device when doing sensitive noise measurements, because this will definitely influence your measurement.

When the beamformer was fully characterized I set out to completely make a custom communications library to be integrated into the back end of the existing Murchinson Widefield Array (MWA) telescope. The beamformer would be placed in the desert near the telescope, controlled by a raspberry pi. The Raspberry Pi runs a python script which could be called directly from the back-end and could set the correct gain/phase delay parameters. Eventually I was able to completely reverse engineer the protocol and implement an entire library for this beamformer.

Because of the fact that there was only one of this beamformer in the world, it was decided that the best use for it

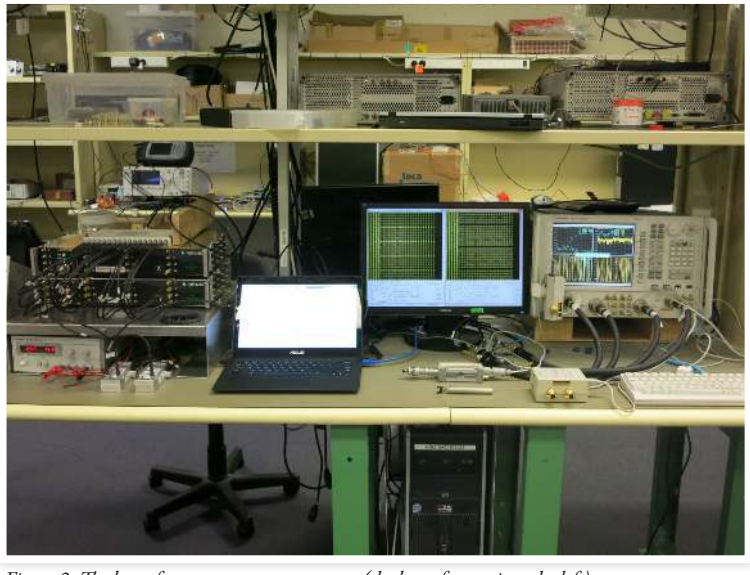


Figure 2: The beamformer measurement setup (the beamformer is to the left)

Figure 3: Laying cables in the unusual green desert.

(other than a 25 kg doorstop) was to use it in an large experimental array consisting of 256 antenna elements, this beamformer would be the last step combining the signals from 16 antenna tiles (which in turn have 16 antennas).

> "We had to continue 400 km off-road to the location of the telescope."

One of the most interesting experiences during my internship was that I actually was allowed to visit the telescope. This meant going from Perth (where the institute was located) 800 km to the north. The journey itself was already an interesting experience. First up was a flight to a city to the North called Geraldton, there we rented some large all-terrain vehicles designed for mining. After some safety briefings and indigenous culture briefings we had to continue 400 km off-road to the location of the telescope. Mostly these expeditions take a week, and the people working on the site will stay at a local farmer for accommodation. During the week I had to mainly assist in maintenance of the existing radio telescope (MWA). This meant replacing LNA's fixing broken antenna tiles, and checking receiver boxes (even doing some weeding around the antennas). All in all it was an interesting experience. Which concluded my work done for ICRAR, and it was time to do some travelling around Australia.

Master Thesis

After a few weeks supervising first year students it was time to start my Master Thesis, the last part before obtaining my master degree. I decided to continue with the area of radio astronomy. Telecommunication Engineering had an assignment in combination with a small satellite company to develop a radio astronomy payload.

The project was a small part of the OLFAR project. The orbiting low frequency antennas for radio astronomy (OLFAR) is a collaboration between ASTRON and universities to create a distributed radio telescope in space using very small satellites as a platform. These small satellites are the size of a milk carton and cheaper to launch into space compared to large satellites. These small satellites have antennas that are designed for low frequency radio astronomy. Because of

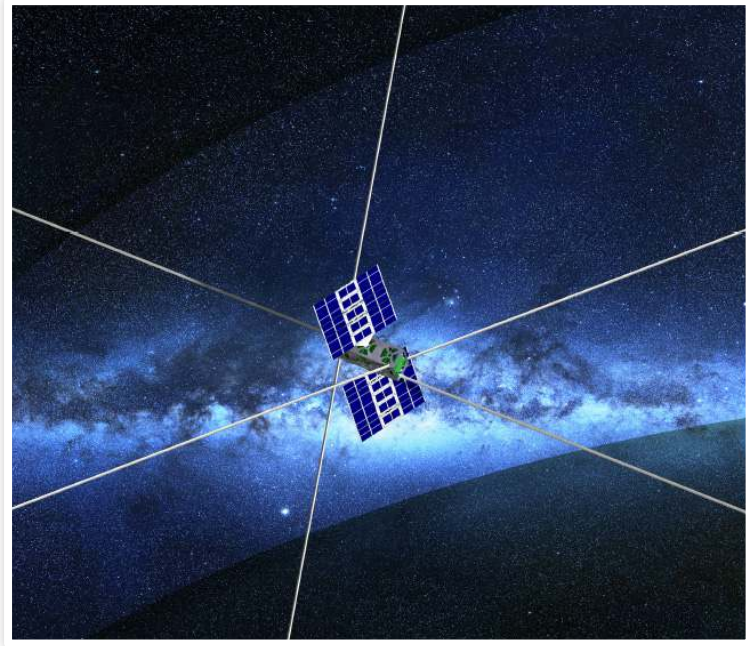


Figure 4: Impression of an OLFAR node

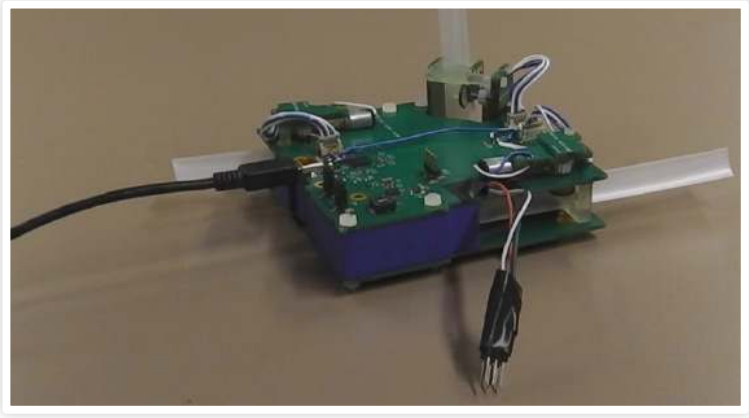


Figure 5: Laying cables in the unusual green desert.

the large wavelengths of these frequencies antenna arrays across large distances are needed. The idea is to create a satellite cluster spanning about 100 kilometers. This satellite cluster is designed to perform distributed interferometry and send the data back to earth to process. The advantage of a distributed system is that it is very robust because there is no single point of failure.

Because each small satellite (also called node) needs their own radio astronomy receiver, I was tasked to design such a receiver. The University of Delft already designed very large expandable antennas that fit in a compact small satellite. So the antenna existed, the goal was to design a system to use this antenna and provide a suitably conditioned signal to the digital processing unit of the satellite.

The astronomical receiver has to work from 0.3-30MHz so very wideband. The first important choice is between amplifying and digitizing the whole band, or choosing a narrowband topology. Choosing a narrowband topology has favorable noise performance and simpler analog to digital converters (ADC). However only a smaller band can be observed at any time. These days ADC's and DSP's are very good so I opted for the wideband solution. It simplifies the entire system to an amplifier in combination with a filter and ADC.
The antennas used are very thin dipoles, so very narrowband. The antennas will have a large mismatch on most of the frequency band, because of a heavily fluctuating impedance across the band. Radio astronomers make receiver sky noise limited. This means that the system is maximally allowed to contribute 1/10th of the available sky noise. The sky noise is very large for low frequencies, so the receiver specifications for these frequencies can be very lenient, making it easier to deal with large mismatches. The resonance of the antenna was chosen in the middle of the band to get an aperture as large as possible (to pick up most signal). A matching network provides reasonable matching for the higher frequency range, because of the more strict noise performance. Finally a fast ADC is chosen, which is also with the power specification. The ADC will have a sample rate of 300 Mega Samples per second, enough to cover a 30 MHz bandwidth.

Unfortunately there was not enough time to realize the design, but a very feasible receiver architecture was designed. After a presentation with some difficult questions I was able to call myself Master of Science! I can highly recommend the master telecommunication engineering for those who are interested in the challenging world of radio and high frequency analog electronics.

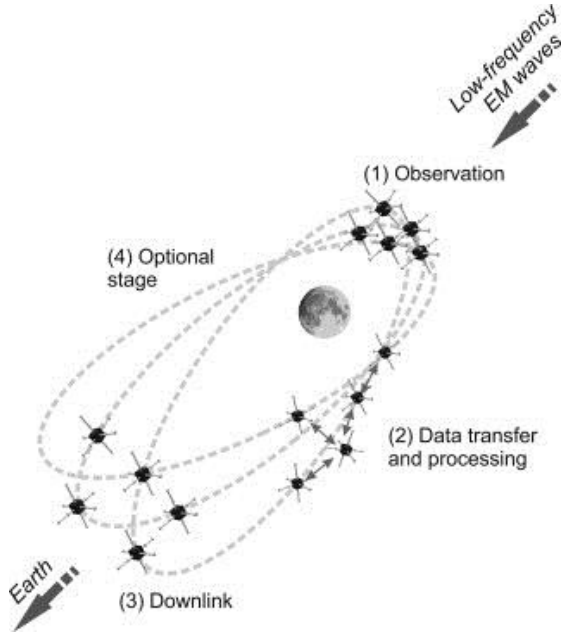


Figure 6: OLFAR Swarm concept.

Solar Team Twente

Starting in 2017

Author: Jan Lenssen

A new team, a new car, and a new chance in Australia next year! My name is Jan Lenssen and since September I have been working fulltime at Solar Team Twente as an Electrical Engineer. I was asked to write a bit about my work here and to tell you what we have done so far. As of writing, in the beginning of November 2016, we are still looking into a lot of different concepts. This means that it is difficult to focus on a single subject, so I thought I could start by telling you something about our new team and the role of the electrical engineers. I will tell you about our last race in September as well. The more technical stories will follow in a later edition, so let's start with my team.

Composition of the team

As you might expect, building a very efficient, but also reliable car requires a team with different disciplines. Although the functions present within the team differ slightly every edition, the general composition of our team is close to the composition of the teams before us. The technical team consists of members from different engineering backgrounds. We have people working on the aerodynamics, making sure the car will experience as little drag as possible (they make it look slick, basically). Then there are team members working fulltime on the mechanical side of our solar car, which includes the suspension and tyres for example. There are also team members that are responsible for the construction of the body. They will make sure the body will have the exact shape that was designed by the aerodynamics team, while it still is strong and stiff enough to maintain this shape during the race.

I myself am part of the last technical sub-team, the electronics team. Compared to previous editions of the team, our sub-team has almost doubled in size. In previous years, Solar Team Twente had two electrical engineers and one member responsible for the data acquisition. The people with these

functions work together closely to make everything around the electrical system and sensor network perform optimally. This year we have four electrical engineers, so what do they all do?

Electronics

My responsibility as an electrical engineer within Solar Team Twente is to make sure the solar car collects as much energy as possible, while using as little as possible. The part that collects the energy includes the solar cells, of course, but also the maximum power point trackers, or MPPTs for short. These devices make sure the solar cells always see the optimal load so that their output power is at its highest. The collected energy goes to the car's battery. Last year, a new part of the solar collector was SABINE, which improved the performance of a string of solar cells by balancing the output of the individual cells. Normally, a string of solar cells is as good as its weakest cell (when a cell is shaded for example), but with SABINE the loss of performance of a single cell can be balanced by the rest of the string.

The solar collector has become an even bigger challenge this year, as the rules have been changed as to only allow 4 square meters of solar panels. Previous editions this used to be 6 square meters, meaning that our expected energy income has become a lot lower.

Everything after the battery is used for spending the collected energy. In the best case, all energy is used only for propelling the solar car towards Adelaide. Of course, in every step between the battery and the road, some losses are expected. The electrical engineers are responsible for this powertrain and must

make sure the car can reach the finish line the fastest. We try to achieve this with as little loss as possible.

A last, but important part of the electrical system is the telemetric system. All parts of the solar car communicate with each other via CAN. The steering wheel can tell the motor controller to go faster, for example. A lot of data is communicated all the time and a lot of this data contains vital information about the status of the car, but also about the speed and power consumption, for example. This is where data acquisition and the electrical engineers work together the most. The guy doing the data acquisition is the one with the laptop that is always standing close to the car. This is something he already got to practice during our participation in the European Solar Challenge, the first race with our team.

European Solar Challenge

At the end of September we had this first race, only a month after having started with the project. We competed in the iLumen European Solar Challenge at circuit Zolder in Belgium and became first! It was quite a special race, as it lasted 24 hours, with only two single hours of charging time in between. Because in Belgium the sun does not shine during the night, we used these charging hours to get the energy needed for racing in the dark.

With little time to prepare, we luckily could count on the Red One and the team behind her to help us win this race. We gained a lot of experience with working as a team. Everyone had their role and together we made sure the race and service stops went very smoothly. I was one of the drivers and got to drive between other solar cars and two Teslas. It was great to see the different strategies employed by the other teams. Some teams were changing their speed a lot, while others were driving on quite slowly, but steadily, hoping that the rest would be unable to complete 24 hours.

During the end of the night, we managed to get the lead and did not give it away, despite the effort of the other teams. The European Solar Challenge gave us insight in the importance of good teamwork and a glimpse of the effort that is necessary to make a winning solar car. Small problems can mean the difference between winning or not. Everyone and everything has to work efficiently and reliably. We have plenty to look forward to.

Prospect

At the moment of writing, the largest part of the project is still ahead of me. During the next couple of months we will start the construction of the mock-up and create the first prototypes of the electrical system. After that, I will be able to tell you a lot more about our new car. In the meantime, a lot of tests still have to be done to find out where we can improve the design of the previous solar cars. Rest assured that our team will work very hard to accomplish our goal, winning the Bridgestone World Solar Challenge in October 2017!

Photos made by Ooms Photography

SOLAR BOAT TWENTE

Author: Heleen Jeurink

Solar Boat Twente is a new student team at our university. You have probably heard of it, but for those who haven't a short explanation: We design and build a boat, solely driven by solar energy. This will be the very first solar boat made in Twente!

The big challenge is to turn the energy from the sun into speed as efficiently as possible. There are a lot of components in the boat, all of which are of high importance in the whole process. See what the boat is going to look like in the picture.

Solar Boat Figures:	
Length	7 m
Width	1.6 m
Cruise speed	35 km/h
Top speed	50 km/h
Weight	110 kg

With this great boat we're going to participate in 2 races: Friesland and Monaco. More about the races later on. For now, we've set ourselves two main goals:

1. Top-3 finish in Monaco
2. Innovation in the 'Solar Boat World'

As a new team, we have an opportunity to use new technologies in our boat, as we don't have anything of past years that we have to use again. This is apparently the best moment for improving the solar boat industry, so we've promised ourselves to utilize this chance. Obviously, we still want to win the race though!

The team

The team consists of 15 students, of which 11 full-timers. All crazy people who want to spend a whole year on this project. As many as 8 different studies are represented within the team. Since the beginning of September, we have a small office in the Bastille. Just enough for everyone. This causes easy communication within the team. Another effect is that we sometimes really can't remain serious. Our new hobby is boat jokes: making as many puns as possible with 'boat' or 'float' or something like that. Really tiresome...

A special strength of our team is the unique collaboration of students from different disciplines, together with external experts, researchers and companies. We only miss maritime students, but we believe this will help us to build the boat without any prejudices about maritime techniques.

Building a boat is not just technical however. The team is divided in 4 subteams:

1. Hull & Hydrofoils
2. Propulsion & Electronics
3. External Affairs
4. PR

All subteams together form a complete team to make Solar Boat Twente a successful project.

How it all started

The whole story started with two mechanical engineering students. One of them, Jasper, had once participated in a solar boat race at secondary school. This was all a bit amateurish, so the time for improvement had come! He set up Solar Boat Twente together with a friend, Hidde, in order to make a better boat and participate in international races.
As soon as the summer had come, the two friends had a whole team of 15 complete. During summer all members finally met each other at the Dutch Solar Challenge in Friesland or at one of the introduction days. Then it was the 5th of September: the team officially started. First week was mainly orientation what is actually inside such a boat, what we have to/want to achieve this year and who is going to do which things. And there were less serious things like furnishing the office and painting our logo on the wall.
Right now, over 3 months later, a lot has happened. The design is already presented and we know how and where most parts of the boat will be made. From now on it's time to put our design into practice in order to finish the boat on time before the first race. Additional effect of all practical work is more space in our office for the ones who stay there .

The race

One of our main goals is finishing top-3 in the world championship in Monaco. But that's not the only time for the boat to race. The first race we will participate in will be the Eneco Solar Boat Race in Akkrum, Friesland. This race is in the last weekend of May 2017, feel free to come by and support us! After this race, there's a few months left for testing and optimizing the boat. Then in July 2017 our main race for this year will be: The Monaco Solar Boat Challenge in, surprisingly, Monaco!
In a solar boat race we distinguish 3 parts: endurance, slalom and sprint. Endurance is a long distance (55km in Akkrum/ 2hrs in Monaco), sprint a short distance and slalom is sailing around buoys. We make our boat reliable to be sure we'll reach the finish, but take some risks too to distinguish our boat from other teams.

Our innovations

So we want to make our boat 'innovative', can we specify this? Sure! The two most innovative parts are: the solar deck and the electronical control of hydrofoils.
About the solar deck: it will be made of thin-film. That's a flexible film which is much lighter, cheaper and easier to make than conventional panels. It is however still a bit less efficient, but there are massive improvements made in the past years. So we want to contribute to these developments by applying thin-film on our boat.
The other one concerns the hydrofoils, they lift the hull out of the water at speeds of 20km/h or higher. These hydrofoils can be controlled electronically, to keep the boat stable, instead of mechanically. Some sensors collect data, which will be used for the hydrofoil control system.

Electrical engineering in our boat

The electronical control of hydrofoils is a good example of where you can find EE in our boat. As already mentioned, we'll make a system in our boat that can measure the stability of the boat and then automatically controls the foils in order to keep the boat stable in pitch, roll and height above the water.

The most important part of our boat is of course the solar cells. These thin-film cells are divided into different arrays and then connected to MPPTs. Next there is the battery box to store energy for later use. Last step is bringing the energy to the electric motor. This motor will then be connected to the propeller, which will propel our boat in the water.
And there are more parts in between solar cells and motor for control and protection of the system, like a battery management system and motor controller. Lastly we have some fancy parts too, like a dashboard that must be made. The person driving the boat should of course know all important information about the boat, so that is to be displayed on a dashboard. The team ashore must know everything too for adjusting the race strategy, so more displays, some telemetry, data-acquisition, the weather conditions must be known, etc...

Get involved

In case you think: 'That's a very cool project, I want to get involved!', just come by in the Bastille. We always have coffee and if you're lucky, even cookies! In a year, so the beginning of 2018, we start looking for a new team. But for now, we only have one EE'er. So some extra help is always welcome!

To eat and to drink more

Author: Céline Steenge

Think about December 22nd, think about the evening, think about the fantastic Christmas dinner of Scintilla!

It has been a few months already but the Christmas dinner is still fresh in our minds. The evening started with standing in line to SCALA in order to get your meat. Luckily, three handsome guys saw that standing in line is not the most fun thing of the Christmas dinner and so the grabbed the piano and started singing for us. Not sure yet whether this was better, but it did give a nice atmosphere.

When everybody got seated, Friso started the welcome speech written on many coasters. On these, a quiz was written! And now we know for sure, members of scintilla are not great with quizzes... Answering the question 'what to do when there is fire' with 'take photos' and 'do we go to the Starbucks' with 'yes', was not the desired response. After the amazing quizmaster finished his speech, it was the president's turn. As a true president, he made a speech about nothing, thanked some people and after a long time cheered our famous scintilla cheer. Now, the Christmas dinner really had started off. Okay maybe one more thing, Camilla and I had the great idea of lighting up by decorating ourselves with Christmas lights. A warning for everyone also wanting to do this, Christmas lights become quite hot and on bare skin, it is not a very nice feeling for a long time.

The first few hours were a lot of eating. Everyone was trying to not get set on fire, but one table was not so fortunate. Since we had such a good quiz, pictures were immediately taken. Also, our fire brigade saw it happening and they were quickly there to stop the fire. Everyone could finish their meal with their third, fourth, fifth or maybe more glass of wine. Due to all this wine, everyone became very talkative. And due to all the sugar in the soda, the people drinking sugar also got their sugar kick. Time to start writing Christmas cards!

It is always a fight among the board members to get the most space on the Christmas cards to write them full with personalized messages. For the members of Scintilla, it is a fight to get the full board and with maybe some space left somewhere also your mommy(s) and/or daddy(s). Of course, also SCALA has its Christmas cards and so the second round begins. Find all SCALA members and let them write a message on their Christmas card for you! The SCALA card is a bit more difficult. First of all due to finding all the people from SCALA since they are with a lot. Second, by finding enough space on the card to let them all write their message! But all of it is done with the Christmas feeling (and maybe because of the wine and sugars).

After dinner, the drink started. People were already very very very nice to each other and this only continued. STRESS also had their karaoke borrel and so some famous sing-a-longs came by. From the drink on, I do not remember very special things happening worth sharing. I think that is a good thing. Let the next Christmas diner be as awesome as this diner.

Wine tasting evening

EEsports ice-skating

Active Members Activity

Sjaarcie laser-gaming

Afterlife

Author: Jildert Ketelaar

As studying is one of the best times of your life, you probably don't want to think about what to do after finishing your study. However, there is a time when you actually should... Luckily, there are a lot of opportunities to think about it, like lectures and excursions to different companies and of course the 'Bedrijvendagen'.

My name is Jildert Ketelaar and I'm 28 years old. I started my study Electrical Engineering at the UT in 2006 and finally graduated four years ago, in December 2012. In this article I will describe how I experienced my study and what I currently do.

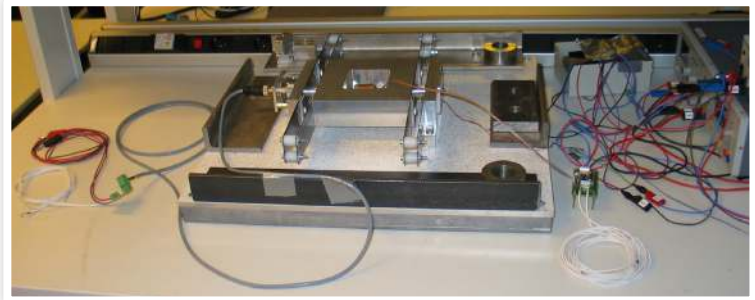
Before starting my study I went to a couple of Open days in both Delft and in Twente. As I grew up in a small Frisian town I did not feel very at home in Delft, but I very much did on the Campus, so this made my choice easy. I found a nice room at the Witbreuksweg and by coincidence, another guy just starting studying EE also just moved in there.

Of course I joined the 'Introductie' period or 'Kick-in' as it is called nowadays. During this period I met a lot of fellow students by means of the 'doegroepen'. In my opinion this is a very effective way to start your study, besides being a lot of fun! In the first months, I did a lot of projects together with people from my doegroep.

By putting quite some time in studying, I managed to finish the first two years nominally. During my bachelor I also joined the student skating association D.S.V. de Skeuvel. In my third year I joined the board of this association and in the year after that I joined the Study tour 'Ngoi Sang' to Malaysia, Singapore, Vietnam and South-Korea. These two non-study related activities cost a vast amount of time, but also taught me a lot of soft skills. Therefore I certainly would have done this again. By combining my Bachelor thesis with the Study tour contract research at Nedap, I was able to finish my bachelor in my fourth year.

In the period between being treasurer of the Skeuvel and the start of the study tour I have also been treasurer of Scintilla for a couple of months. This demand arose as the 'board change', which occurred two times a year, was changed to once a year. During almost my whole study period I was also a member of the BinEx/SLC committee, which name changed to LEX somewhere in the past years. I organised quite some company lectures and excursions which was always a lot of fun to do. I must however say that later on I did not really look for a job at one of the companies involved.

After my bachelor I started my master at the Control Engineering chair (Robotics and Mechatronics). I doubted between a master in control engineering and embedded systems, but the connection between software and hardware attracted me more at control engineering. Also, my master courses went quite well and in my second year of the master I did my internship at Mecal in Enschede. Among other subjects, the department where I was involved focussed on Vibration Isolation e.g. for accurate machinery. I worked on a vibration isolation platform where a displacement sensor, able to measure low frequency vibrations, was combined with an accelerometer, which was used to measure more higher frequencies. I succeeded to make this test setup work. It was very nice to put a cup of coffee on the platform, shake the table the setup was placed on, and not seeing any vibration occur in the cup.



Test setup internship at Mecal

After finishing my internship the time had really come to perform a graduation project. I did this at the Robotics and Mechatronics chair. A previous graduation student had designed and made a robot where the knees were actuated by 'Variable Stiffness Actuators'. These actuators had internal springs with the purpose to capture energy during the landing of the feet and to use this energy later on. My task was to design a controller for this robot. I researched different control strategies and designed and implemented one on the robot. Unfortunately, in the end the robot was only capable of walking a few steps, but I learned a lot about different control strategies and I had a good time working on it.

Except for visiting the 'bedrijvendagen', I did not actively search for jobs during my graduation project. I knew that there were quite some companies looking for Electrical Engineers, so I did not worry a lot about it. I was also asked to perform different PhD assignments, but as working by myself during my graduation was not that fun, I decided not to do a PhD. Via one of my fellow graduation students at the chair I was contacted by a recruitment agency. I was always a bit reserved against these agencies, but they easily introduced me to different companies and within two months after my graduation I was invited to work at two different companies. As I wanted to work in the field were software and electronics meets hardware (i.e. Mechatronics) I ended up at VDL ETG in Almelo, a high tech machinery factory.

VDL ETG used to be a machinery factory of Philips. In 2006, VDL (also known for building buses, also the ones in Enschede) acquired the factories in Eindhoven, Almelo, Singapore and China from Philips. VDL ETG designs and builds high tech machines or sub modules for the Semiconductor, Healthcare and Solar market. As a mechatronics designer I'm involved in different design projects for customers like ASML, Zeiss, NXP and Philips Healthcare. The fact that both the design and the construction is done in-house, makes my work really hands-on. The mechatronic concepts and components like sensors and actuators which we select and design, are integrated a couple of months later in our cleanroom.

Another part of my job is to support our factory during qualification of machines and submodules. When a module does not completely fulfil the customer specifications, we dive into the issue and do all kinds of checks and measurements to pinpoint the problem. These measurements can for example be transfer functions or hysteresis measurements. As VDL ETG builds the ASML Waferstage, I've also been to ASML multiple times to support the qualification and integration over there.

Besides working at VDL, I also joined the 'Nationale Reserve', a reserve corps of the Royal Dutch Army. Its task is to protect and secure in the event of a disaster or crisis on Dutch territory. I already started to do this during my study as a hobby and to earn a little money. After a couple of years in the rank of soldier, I did different courses to become an officer. Since last June I'm now Platoon Commander in the rank of Second Lieutenant. As my regular daily job is purely technical, the reserve army has given me a lot of opportunities to develop my soft skills. Furthermore, you visit a lot of places where you normally would not go. Examples are the 'National Security Summit' in 2014, 'Prinsjesdag', the Nijmegen four day marches and the coronation of Willem Alexander.

Currently, I'm still happy working at VDL ETG. If anyone is interested in doing an internship or graduation project please feel free to connect me, this applies also for when you're interested in the reserve corps!

Internship at MediaTek:

How to debug a complete smartphone transmitter

Author: Joep Zanen

It wasn't until the end of the lecture that I realized that it had been the very last lecture of my studies. My time as a student is slowly nearing its end, but as one of the remaining parts of my last year as a student I still had to do an internship. Via contacts of the Integrated Circuit Design group I ended up at MediaTek as a design verification engineer. MediaTek is a Taiwanese semiconductor company, mainly active in making chipsets for smartphones, tablets and smart TVs. Worldwide, the company has about 10,000 employees. For my internship, I now work at the office in Kings Hill, England, in the middle between London and Dover. Here, a team of about 30 people work on parts of MediaTek's chips that deal with wireless communication, specialized in transmitters.

The team I work in is the Design Verification team, currently a team of three. Our job is to make models for every circuit to test the integration of the complete signal chains for both digital and analog signals before the chip will be manufactured. This includes everything from the chip's power supply and RF circuits to its digital controls. The work thus consists of two phases: modelling and top-level verification.

> "Why do we need design verification?"

Why do we need design verification? Over the last decades, microchips have grown more and more complex. Especially in the smartphone industry this complexity is twofold: not only in the increasing size of processor power and memory, but also in increasingly complex RF circuits with multiple transmitters and receivers, many hundreds of digital inputs and controls, feedback paths and calibration loops. Back in the early days when a cellphone had a small processor and a GSM circuit, it might have been possible to run a simulation of a data transmission, but this isn't the case anymore. Not only do we want to simulate a transmission: we are especially interested in the mixed signal paths which e.g. automatically scale output power up for better transmission, or down for lower power consumption. To simulate this with a standard analog simulator, an enormous system would need to be simulated with a small enough simulation time step to properly deal with RF signals. In this approach, not only the RF circuits have to be simulated with this small time step, but the full design will

> "As a result, it will take months for a single simulation on an RF circuit, if not longer."

be treated like this. This means even the blocks which are not really interesting to simulate at these frequencies (e.g. the power supply regulators) will become very computationally intensive. As a result, it will take months for a single simulation on an RF circuit, if not longer. If we remember our first year courses correctly, you should have noticed that digital simulations of your VHDL code generally were a lot faster than simulations of your analog FM transmitter in

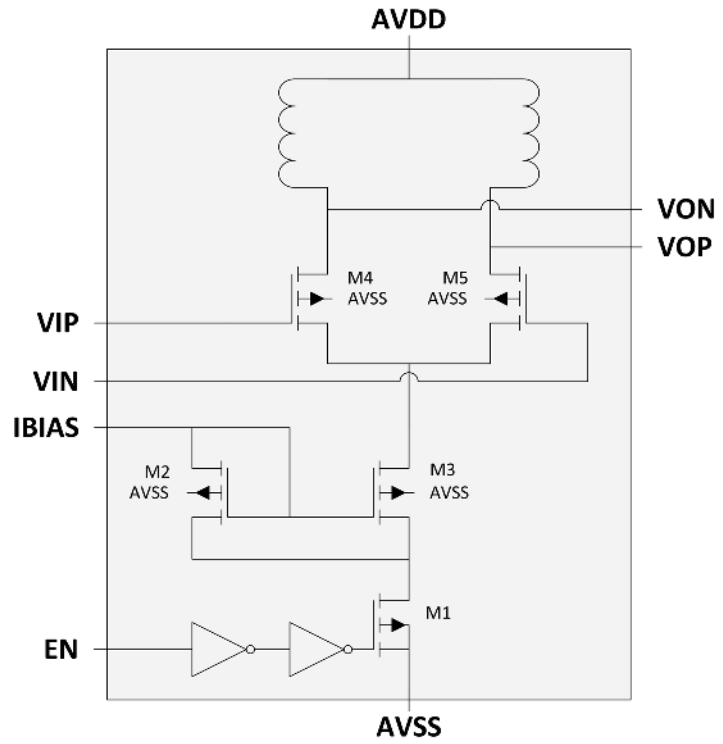


Figure 1: RF-amplifier circuit

> "The result of the mentioned advantages is enormous."

LTSPICE. There are three main reasons for this. First of all, the complexity of the system is drastically decreased in a programmed model. There are much less internal states with much simpler relations between them. Furthermore, a digital simulation only needs to simulate a piece of code if one of the variables in its sensitivity list changes: parts can thus be simulated individually and run on their own time step. Lastly, analog simulators need very small time steps to simulate RF frequencies, especially with the modern square wave oscillator architectures. Digital simulators only run a time step when the input changes, and this is only two times per period for a square wave.

The result of the mentioned advantages is enormous. It is realistic that modelling for digital simulators allows for a simulation with:

- A hundredth of the internal states
- A hundredth of the dynamic relations
- A tenth part of the system that needs to be simulated per time step
- A hundred times coarser time step

The first and last of these conditions lead to a reduction in required memory of a factor 10 000, the latter three lead to an increase in computation speed of a factor 100 000. This is the difference between a simulation of a minute, and a simulation of more than two months and allows for top level simulations of the complete analog part of the SoC, together with its digital control. Wouldn't it be great if we could simulate analog circuits using a digital simulator?
This is where the verification engineer comes in. My job is to make so called 'wreal models' in Verilog (a hardware description language). 'wreal' refers to a floating point data type for wires between functional blocks as you know them in VHDL. These floating point inputs and outputs of a block mimic the analog behavior, while still allowing for the use of a digital simulator.

My job starts with an analog circuit and a document stating a description of what the model should do: the model specification. An example of a circuit as you might find in an RFIC is the differential amplifier in Figure 1. Typical for integrated these RF circuits in a large system are the inputs for bias currents and enable signals, used to save power. The circuit needs a differential input voltage between v_{IP} and v_{IN} and generates a differential output voltage between v_{OP} and v_{ON}. An explanation of the circuit: M1 is a switch to enable or disable the circuit, driven by a double inverter buffer. M2 and M3 form a current mirror, generating a bias current from a reference current at i_{bias}. M4 and M5 form a differential pair, converting the input voltage to a current. The inductors function as high impedances at RF frequencies, and convert the differential current to a large differential output voltage. You can also take a more abstract look at this circuit: if the supplies and bias are correct and the device is enabled, system behaves as an amplifier with certain gain. From a system point of view, this is all we want to know about the schematic.

This system level information is summarized in the model specification and is the basis for the Verilog model. It states what the required values are for the supplies and biases and what the system level behavior is. In this case the behavior is simple: amplification. There are however cases, such as frequency filters or blocks with many digital inputs for different settings, which are much harder to model. The wreal equivalent of the schematic in Figure 1 is given in the pseudo Verilog in Figure 2. This model shows the same system level behavior as the circuit, but you can already guess that it is much faster to run these few lines of codes, than it is to simulate the complete transistor circuit.

> "In most of these cases this is due to errors in the control sequences or the models."

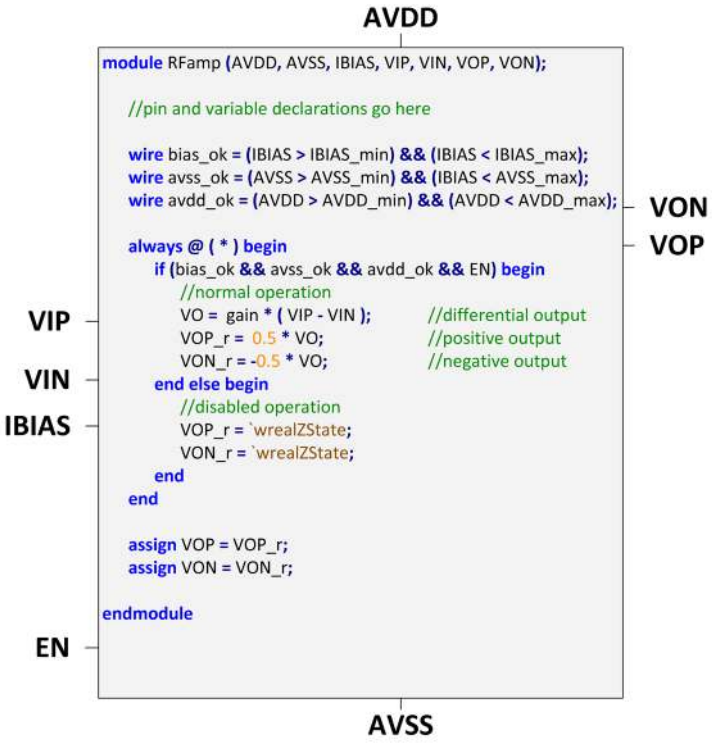


Figure 2: RF-amplifier model

Once the modelling phase has passed and there are models for every circuit in the system, the cosimulation phase can begin. In this phase, the complete analog system and its digital control will be verified. An example simulation would be the verification of the programmable system gains and the corresponding digital settings. Ultimately, these settings are controlled by a digital controller. Thus, a programming sequence has to be written to test the complete system. After simulating, the wreal signal can be traced through the transmitter blocks and it can be checked whether the system behaves to its specifications. Quite often it does not. In most of these cases this is due to errors in the control sequences or the models, but sometimes smaller or larger problems in the system pop up. Using these simulations we discovered, amongst other things, that the transmitter clock phases were generated in the wrong order, and that a calibration algorithm uses gain settings which are not supported. By using this method however, we found these issues in time to change the design.

> "When writing the control sequences and running the cosimulations, you also learn how all blocks fit together."

By making models for the schematics, you learn the behavior of every part of the system, down to the transistor level.

When writing the control sequences and running the cosimulations, you also learn how all blocks fit together. In the end, you have a very good overview and deep understanding of a state of the art smartphone transceiver. Though these jobs are not actual analog design, it is still a highly interesting job as an analog designer.

Two awesome worlds

Author: Ankie Kuiper

The world of Scintilla and my usual world in Rotterdam are two complete opposites. Three and a half year ago I first visited the Zilverling and I was in a shock due to what I saw. Students were gaming during their lunch break. Never had I seen this: the complete dedication of playing Worms and Minecraft, while quickly eating lunch and getting free Scintilla coffee. Where I usually spend my lunch breaks talking to friends, I was astonished by this Fantastic phenomena.

This is not the only difference between my student life and that of an EE student. In my study: Health Sciences, proximally 90% is female or 99% when we look at attendance. In my study association the percentage of males is luckily a bit higher. We still find it an achievement to have two male committee members, but the mix is a lot better than in the lectures.

In contrast most of the EE students are guys. The few female students have a luxurious position with an overwhelming amount of male attention. Even I as a guest never had more male attention, than during a Scintilla drink.

However that is not the reason why I love to be at a Scintilla drink. Of course the Grolsch beer is really nice. The ambiance is great. And the people at these drinks are even better. Over the years I had so many good conversations and memorable nights with Scintilla members. I am enormously jealous of your own bar right under the Scintilla room. I cannot imagine any place that would be better to grab a drink. Unfortunately the Erasmus University never really followed this fantastic idea, but luckily I can sometimes enjoy this with you in Twente.

Never had I seen this: the complete dedication of playing Worms and Minecraft, while quickly eating lunch and getting free Scintilla coffee.

Your "own" bar has a big advantage: fantastic constitution drinks. During my board year at the FBMG I have been to a lot of awesome constitution drinks. However nowhere were the board, guestbook and pedel better protected than at Scintilla. In Rotterdam my board and I were fanatic and trained to steal from

> "Sometimes Scintilla inspires me to organize or improve my own association."

other associations, with blood, sweat and tears. So we came in the AbScInt with courage and hope to at least steal the guest book. However when we saw the wall of protectors (or pedellen as you call them) we soon lost the hope. Instead we had a great night with drinks and conversations in your bar.

Not only the locations of drinks differ, but the behaviours during drinks over the night too. When the night progresses in Rotterdam more people start dancing. At the end the whole dancefloor

> "Nowhere were the board, guestbook and pedel better protected than at Scintilla."

is full. In contrast I rarely see anyone dance at a Scintilla drink. However you use karaoke to lose your last energy. Full devotion you perform songs from frozen or queen. However, both dancing and karaoke are a great end for a drink.

I could continue summing up differences. But there are also a lot of similarities. In both worlds are students that made friends due to joining a committee, doing a board year or meeting at activities. In both worlds students learn a lot from going to activities and being an active member. In both worlds students enjoy the best part of their life.

The nice thing is that we also can learn a lot from each other. Sometimes Scintilla inspires me to organize or improve my own association. For example I use

> At the end the whole dancefloor is full. In contrast I rarely see anyone dance at a Scintilla drink.

your fantastic cantus as an inspiration for the FBMG lustrum cantus and introduced "schoenzetten" (sinterklaas) in the FBMG board room. In addition Guus sometimes learns from my FBMG stories.

In the last 3,5 years I became to love Guus' world in Scintilla. It took some getting used to from both sides. I needed to adjust my conversations and sometimes change my behaviour and some of you needed to get used to the strange girl from Rotterdam that was at Scintilla really often for some weird reason. But in the end you took me in and accepted me, for most as the girlfriend of the president and for some even as Ankie.

Ankie Kuiper
Student Health Care Management
Erasmus University Rotterdam
Old board member FBMG
Guus' girlfriend

Junction

Author: Maarten Thoonen
Mark van Holland

Daphne Boere studied Biomedical Engineering, lived in Germany for a while, became lab manager and research assistant for thr Biomedical Engineering group and is now study advisor for Electrical Engineering. In this article she tells about what she has done in the past and what she does now as study advisor.

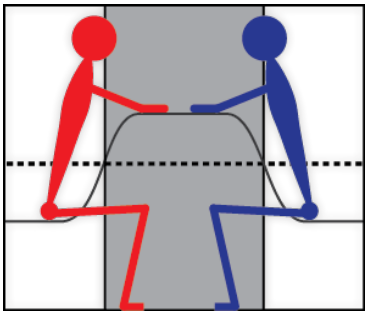
"I was born in Cuijk, a village in Brabant next to the Maas. I grew up there and lived there until I was eighteen years old. Then I started studying in Enschede, where I did Biomedical Engineering. I started in 2002, so that was the second year that programme existed. I finished my bachelor's and my master's here, and then I moved to Munich with my boyfriend, now husband, Ruben. He went there because of his job, and the goal was that I would find a job there as well and that we would live there for about three years. But as I was unable to find a job, we decided to go back after a year. Or actually, I got to choose whether we stayed or went back, and I chose to go back. I wanted to go back to do a PhD, so I did that for four years. I did not finish my PhD and did not earn the title, but I did successfully finish the project for myself. Then my contract ended, which is usual for such contracts. Then I became a lab manager and research assistant for CTW Biomechanical Engineering group. I had a contract for one and a half years, and unfortunately there was no extension possible, otherwise I would've liked to do that a little longer. Then I heard there was a vacancy for study adviser, and I thought, that it could be a fitting job for me. I could help students by using my own experience, and be useful for people. That was also why I chose Biomedical Engineering, to help people. So now I am the study advisor for Electrical Engineering and it suits me very well."

For the people who never had to meet you: what exactly does a study advisor do?

During my studies I also actually never had a need for the study advisor, so when I did the job interview I got the question 'what do you think a study advisor does?' and I didn't really have an idea. But a study advisor, for instance, advises students on what is the best way to continue their studies when they got a delay of any kind, like not completing a module due to illness. You can contact me when you encounter issues that have an impact on you study and then I can help you to solve the matter or set up a plan (and guide you if necessary) to tackle it.

What did you do when you were in Munich?

First, I did a course on German, so I'm now relatively fluent in German. I did that course because I initially couldn't find a job, and I thought being more fluent in German would be helpful. The course was two months, and when



I couldn't find a biomedical job after a month I decided that this wasn't it, and that I wanted to go back. But as my husband had a contract for a year, I decided to find something to do until that contract ended. As I could speak both Dutch and German, I started searching for some translation jobs and I found two. So now there exists a CD with my voice on it, pronouncing Dutch words for a Dutch course for Germans. I also worked for a pet shop, which wanted to have a Dutch web page.

Why did you start studying Biomedical Engineering?

Not sure if this happened for more people, but my mom found an advertisement for the study in the newspaper, and asked me 'hey, wouldn't this be something for you?'. And it was. I always wanted to do something with people, specifically children, be a children's doctor. But I discovered that I didn't really like biology, and my mom told me that studying for that would involve memorizing lots of things, which I also dislike. In high school, I had a 'natuur en techniek' profile (mostly physics and math subjects), and I had the subjects math B1 and B2, and I kind of liked those. I

looked in Leiden for a math studies, and also here at applied mathematics, but designing security systems didn't seem all that interesting to me. So when my mom showed the newspaper ad to me, I saw that it was the perfect combination of helping people and 'beta' subjects.

What kind of internship did you do?

I did my internship in Iceland, at the company Össur in Reykjavik. There I researched using literature the best specs of a knee prosthesis. They made a mechanical prosthesis, but there are also electrical, microcontroller-driven prostheses available. They wanted to have a scientific answer to what kind of prosthesis was the best at mimicking a real knee, hoping that it would be theirs, of course.

What kind of student were you?

When I lived at my parents, my curfew was around half past twelve at night, which was about the time the fun started, so therefore I didn't bother to go out. So when I left the house at 18 I thought to myself 'well, nice, now my parents can't tell me what to do anymore'. I really wanted to live on campus, and I started living at Campuslaan 43. The people living there certainly liked parties, so they took me with them. So I went from a good, decent girl, though I think I still mostly am that, to a bit less good, more outgoing girl. I did manage to always be present at half past eight at the lecture on Friday morning, but I wasn't always awake during those lectures. All in all, I'd say I was mostly a serious student. I managed to pass all my first year's subjects. I finished my studies in a bit less than six years, while going to as much parties and activities as possible. During my time at the UT as a student I also played badminton at DBV DIOK. I still play there, and as I got my trainer/coach license there I also give trainings. My husband also studied at the UT, starting with Business Administration and then Mechanical Engineering. He also played badminton at DIOK, and that is where we met. He also still plays badminton, but not at DIOK anymore, he plays in Oldenzaal. He has had a job in Germany ever since we left for Munich, and when we moved back here he started working in Münster at Imtech. Currently he has a job at their competitor, which was called Bilfinger. I'm not sure what it is called now, it is something weird (After some checking the name turned out to be Apleona). At that company, he is a project manager for energy management for other companies. An important customer of them at the moment is FrieslandCampina. There they research their heat (and cold) transport, and try to find ways to improve it. So he also has coworkers who are Electrical Engineers. I also started rowing in my first year, but I stopped doing that after a year and a half. I did continue to be coxswain, though.

Daphne Willemijn Boere

Age	32
Favorite food	Pancakes
Favorite Color	Scintillared or purple-red
Favorite Drink	With alcohol: Baileys Without alcohol: tea

Apart from badminton, what are your hobbies?

I have a large hobby in my 2-year-old daughter, Eline Willemijn. She is named after me and her grandmother. Currently, I'm pregnant again. My second child is due for mid-April. It is probably informative for the students to know that I will be on maternity leave starting from March 9th, and I will not be back until somewhere in the middle of the summer.

I used to do a lot of arts and crafts. I have a sewing machine, which I use(d) to remake all kinds of things. After having Eline that died down mostly, but nowadays I do coloring and pasting with her. I also used to play the violin, but I stopped doing that when I came here to study. I did start again later on, but the violin now lays on top of some closet, so I can't really say I am actively playing it anymore. As a replacement, I sing a lot (of lullabies). My husband and I also did mountain biking for a while, but the bike is for sale on Marktplaats now, so that stopped too. Other than that, I like cooking/baking and eating afterwards, and we recently picked up making large jigsaw puzzles.

What is your opinion on TEM?

I have to say, when they first started with it I was more of a bystander, and I thought "I'm glad I don't have to study anymore" and "why would anyone come to study at the University of Twente anymore?". At my last job, I also was a first years' mentor I still thought about it that way, and even now I pity the students that it is all or nothing, 0 or 15 EC. But now I have also heard the other side of the story: all the subjects are linked to each other, you get math that is actually applicable to the stuff you are working on in other subjects and you have smaller tests every few weeks instead of having to learn everything at once every eight weeks. So now, I also can see the benefits, but I'm still glad I have already finished my studies.

If you could change anything about it, what would it be?

I would make it easier to get a reduced workload. I did a number of committees at DBV DIOK, and that is extra work. Nothing full time, but once in a while it was nice to be able to do two subjects instead of three at the same time. With TEM, that is not possible anymore. On the other hand, if you would make that possible now, you lose a large part of the idea of TEM. But maybe if a student did other things next to his or her studies and could prove that therefore he or she is not available 100% of the time, some exceptions could be made.

What keeps you awake at night?

Our heating system makes banging sounds at very cold nights. And if you try to close the radiator, it doesn't fully close so it makes whistling noises. Other than that, my daughter when she cries, and worries about my loved ones.

What do you want to do in the future?

I hope to be a study advisor for a long time, as I really like doing this. I hope to visit Iceland someday again, so I could see the midland (Landmannalaugar). When I did my internship there it was winter, and it wasn't accessible anymore due to the weather, so that is still on the bucket list. Another country I'd like to visit is New Zealand. Australia is off the list because there are way too many spiders there. Also, I'd like to grow old.

Is there anything you want to say to the students?

Do things you like doing. Find in yourself things that make you happy and do those things.

There also is something more practical which would be useful to put in The Vonk:

Since the start of this academic year, student psychologist Renée Zomerdijk has walk-in hours for students every first and third Tuesday of the month for all EWI students. She can be found in Zilverling, room A102 from 12.30 to 13:30.

The goal of the walk-in hours is that Renée does a short scan and gives the student advise on how to continue. This could be a referral to regular consulting hours of the student psychologists, an external instance, a study-stimulating group, a meeting with a student counselor et cetera. The nice thing about these walk-in hours is that students can get advise. EWI staff can also use these walk-in hours with Renée for advice concerning student mentoring, in case there are (or seem to be) issues. Students do come before staff, though.

Threading the line.

Author: Jippe Rossen

It's Thursday morning 12:21PM, when all of a sudden the lights start to flicker. Annoyed you look up, but only just for a moment. In your mind a stern voice echoes: 'Focus, You cannot be distracted by anything!' Dedicated you resume with the tasks at hand. Meanwhile distant cries of despair fill your surroundings, yet they are barely noticed by anyone. Zero hour is just 9 minutes away. The constant stress on your senses makes your eyes lose focus. Disoriented you look up. Through the blur, you only barely discern the person that walks straight at you through the aisle.

Is this the beginning of some horror story? Well it could be, but in this case it is not what I was getting at
.
The person stops right beside your desk and says: "Remember guys, you only got 8 minutes left, finish up your reports and make sure you hand it in on time!"

> "Being a student assistant feels like being a cord dancer who is threading a line."

I would not be surprised if some people reading this would actually find the situation described above all too familiar. Long hours, the hard deadlines and all those small technicalities to remember do not make it any better. When you are completely stuck and seek help with a student assistant, only to get a cryptic response at best, it might very well lead to a nervous breakdown. But what does a student assistant do? And what are the motivations for their behavior and advice? You may or may not have had these questions before, but in this article I am going to try to make it a little bit more comprehensive, or at least justifiable.

As the title of this article readily says, being a student assistant feels like being a cord dancer who is threading a line. In many ways you have to balance right between two undesired situations. To make it all that much harder; the location of where this line is, is also very dependent on the student asking the question. When the students also work in pairs, it is sometimes just simply impossible to get it right.

> "These are the times where you can be creative and amuse yourself by taking ridiculous examples, whilst still giving very valuable information."

As the job description states we are, just like the ones taking the lab, students ourselves. This means that we know the road of torture the students have to endure. The first base instinct is therefore to help everyone as much as possible. However, do you really help students by helping them as much as possible? You can probably already guess the answer; no...

> "Another approach is to start from nothing and to guide a student towards the right answer step by step."

You might help students out a lot by leading them straight to the right answer. But if they do not learn the underlying theories, you possibly have just wasted their time (and quite frankly you own as well). It is also very unlikely that this will help them with their tests, as these are never the exact same exercises.

So the trick is to give them just enough information to be able to deal with the problem at hand. The problem is, what information to give? And, where to start and on what level of expertise? These however are not the only challenges: Even

at explaining the problem at hand, multiple approaches can be used.

The most 'safe' way would obviously be to relate the problem to the lectures as much as possible. But if a student already got the required tools presented to him during a lecture and still gets stuck, this might just be a dead end. Also, this approach is very time consuming and delays are not something to be thought of too lightly.

> "All the cheesy lines about 'only really understanding something when you can explain it' are all too real."

Another approach is to start from nothing and to guide a student towards the right answer step by step. Note that in this case you use the material of the lab rather than the material from the lectures. You do have to be careful on what to ask though, too easy, or too difficult questions can very easily annoy people, which distracts them from actually thinking about the material. Another hurdle that may occur is that the student may be too focused on the problem at hand. Therefore, you could opt with starting from the basics anyhow, just to pull focus away from the problem at first and to show the bigger picture.

> "This process of decision-making is one of the key learning goals of any engineering degree."

All the stuff above almost makes it seem like being an assistant is worse than being the student. There are of course also good things about being an assistant (other than being paid). You are really forced to be flexible. Often examples or analogies are required to get something across. These are the times where you can be creative and amuse yourself by taking ridiculous examples, whilst still giving very valuable information. One of my personal favorites is explaining how to write a lab journal by doing a (hypothetical) experiment on how far you can stick a pencil up your nose. By giving a ridiculous example, it is much more likely to get through and it may also be easier to remember. (And if the student does not think it is funny at all, you might get the same result out of sheer annoyance.)

Other stuff

Up till now only lab assisting has been considered, but there is more to the job. With the introduction of the Twente Educational Model (TEM) projects are more common than ever. During these projects students have a lot of decisions to make. As it is their project, you want them of course to make their own decisions as much as possible. This process of decision-making is one of the key learning goals of any engineering degree. Sometimes however they do not have the time or knowledge to decide themselves. In that case, you must make the decision yourself. As you do not want to be the cause of their entire project failing, you try to be on the safe side as much as possible. You can always make a project more elaborate or difficult. To simplify a difficult concept is a lot harder.

Assisting projects is altogether much less stressful. The fact that there is no clear-cut answer or sometimes even a goal makes it much more relaxed. It also seems that students see connections between concepts much sooner than with the lab. This once again proves that it really is advantageous to actually prepare the labs (and not only to save some time).

> "Another hurdle that may occur is that the student may be too focused on the problem at hand."

Altogether it is a great experience to be at least an assistant once. It forces you to approach the material in a different manner. All the cheesy lines about 'only really understanding something when you can explain it' are all too real. As in every part of an engineering education, trade-offs are always to be made. It is quite challenging to judge the situation with very little to go on. However, seeing the look on someone's face when understanding some though material or concepts after hours of struggles, really is a great feeling. If not for this or for the money, at least you can get some retribution from all the horrors from the past.

Scolumn

Author: Jaimie Jellema

Hello everyone, I am Jaimie Jellema also known as that guy that does two studies, because I study both electrical engineering and technical computer science. You might wonder, why would anybody ever want to do two studies? Well I was a bit at odds whether to choose computer science or electrical engineering. I knew I would probably enjoy them both a lot, but which one would be more suited. I choose EE, when all of a sudden I was thinking, why not study both? Some emails later, I became a human guinea pig to try if it was possible to do both studies.

I really enjoy doing both studies, people are really nice at the UT. What is surprising is how people differ between studies. I was once told that the difference between EE and TCS is that EE has slightly crazy people, and TCS has either `normal` people or completely crazy. I can confirm that this is true. TCS is not just programming, but some of the TCS people really love their programming.

> "I became a human guinea pig to try if it was possible to do both studies."

While there are plenty of EE people who don't like programming, its wonderful to be able to combine both studies and to design something that is on the edge between them. Take an Arduino, you can hook up your own custom radio communication circuit, and some motors. Program the Arduino, and all of a sudden you have your very own little rc car.

I get asked a lot what it is like to do two studies at the same time. I don't really have a good answer to this. Everything is new for me at this university so I can't really say what is different, because it all becomes so normal to me. It is more intense than doing one study. Time management may be the biggest difficulty in doing two studies. During the first week if I looked at my schedule, I was wondering how could I possibly be at all those places at the same time. But then as time went on you learned what was really important, and what could be done later.

It seems so simple, just go to the lectures of the subjects you are struggling with, and don't go to the ones you find easy. In reality we can surprise ourselves very much, sometimes about how wrong you where about something you thought you knew very well. Or how well you know something that seamed very difficult.

Another big hurdle with doing two studies, is making sure you are strong mentally. You will get pushed around a lot. No matter how hard you try to plan things, I manage to keep to a schedule 2 maybe 3 days in advance. Before things start to pop-up. Obligatory sessions, team members falling ill, things taking longer than you expected. Doing two studies just means having those things twice as often.

People ask me if I have a live, because two studies means a lot less time to spend on other stuff.
All I can ask for that in return is why do you study? Because you want a good job, good life? Or because you enjoy learning? I enjoy learning new stuff, and my study is doing the things I enjoy.
Your study takes probably 5 to 7 years of your life. You should enjoy not just the parties, the sport activities, but even the study itself. The lectures and the exercises. I don't do studies because I have to, but because I want to. That is the reason why I am able to manage everything.

On Location: ASML

Author: Gino Van Spil

On the 13th of October, a group of Scintilla visited the ASML campus in Veldhoven. ASML makes photolithography machines and is the market leader in this field, so I was very excited to visit their campus.

After being received with some much-needed coffee, a short introduction lecture about ASML was given. In this lecture they gave some basic facts about working at ASML. It was made clear that most people have a fixed contract and that around 8800 employees out of the 14500 work at the ASML campus in Veldhoven. Another interesting fact was that just like our study most employees are male. Besides that, we were also told that most of the machines they manufacture are sold outside of Europe. Most go to America and Asia. The machines ASML is currently making are two years ahead of the competition.

In a second lecture the core activity of ASML was explained: designing and building photolithography machines. These machines are used to project the design pattern onto a photo resistive layer on the wafer. After that, the projection layers are etched away, but this is not part of the machines of ASML. To create a modern chip, the same wafer will have multiple exposures with different patterns. Sometimes as much as 50 exposures are needed.

After this second lecture, we got a tour around their campus. At first they gave us a look at a regular working space. In these working spaces no one has their own personal desk anymore, which greatly reduces the mess, since no one can leave their stuff lying about anymore. The tour guide also stressed the importance of coffee machines, as within ASML they function as a place where spontaneous meetings happen. This turns out to be so important, that there are whiteboards near every coffee machine. We continued through some long hallways and climbed some stairs where we were shown a massive space full of cabinets with machinery in them. These are used to filter the air for the 40000m2 of clean room ASML has.

Next we walked to the production facility. Although ASML puts a lot of effort into researching the next steps in semiconductor production, the production facility is an important part of ASML, since stepper machines are made for customers. On the way to the factory our tour guide noted that one complete machine could take up 6 jumbo jets to be shipped to their customer and that it is also important that they are kept at the right temperature during transport. The factory also consists of clean rooms. In these clean rooms the parts of the machines are assembled. They use clearly labelled tools to distinguish tools that are

> one complete machine could take up 6 jumbo jets to be shipped to their customer

'clean' and can be used in clean rooms, and 'dirty' tools. Further in the factory a room full of lenses for their deep UV system was shown. These lenses are used to project the image of the circuit onto the wafer. Lastly we were shown a cabinet about the size of a server rack. One cabinet contains one amplifier and a single machine has multiple of these cabinets.
After lunch we visited the ASML experience centre. Here we had another introduction on the activities of ASML. In this introduction we were told that for 80% of all semiconductors made worldwide, in at least one production step an ASML machine is used. Next there was an exhibition with the visualisation of overlay, which is the measurement of how accurate the different layers in the microchip are placed on top of each other. Then they showed us a video about their EUV (extreme ultra violet) systems. These systems use a wavelength of 14nm to make even smaller feature size possible. Instead of lenses to focus the light, EUV systems use mirrors to guide and focus the light onto the wafer. These mirrors are made with an incredible precision, if one of these mirrors were to be scaled to the size of Germany, the largest bump would be 1mm high.

These systems use a wavelength of 14nm to make even smaller feature size possible.

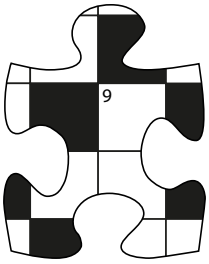
Besides this, there were also some real sized parts on display. The first part that drew attention was a parabolic mirror used in the laser for the EUV system, which is used to focus the light from the laser and guide it to the next mirror. Next to it there was an optical system, consisting of lenses which are used in machines that use deep UV. The last two parts that were shown were the wafer handler. This part of the machine ensures that the right wafer is picked up and placed at the right place in the machine and the wafer table, which is the surface the wafer lays on during exposures.

The last part of the day consisted of a case study about cleaning the wafer table. Despite operating in a clean room, some particles can get stuck on the wafer table. These particles can come from the wafer itself, but can also be a particle from something else. The problem with particles getting stuck on the wafer table is deformation of the wafer. Although the wafer of silicon looks solid at microscopic level, it is not. Due to the particles, the wafer has 'bumps' in it, reducing the accuracy at which layers can be stacked onto each other. The goal of the case study was to come up with a method to get the particles of the wafer table.
After the case study we had some drinks with ASML employees, and finally we went home, another two-hour car drive back to Twente.

Puuzle

Author: Truusje

The winner of last edition's puuzle was nobody! Because nobody sent Truusje a nice new sticker. For this week Truusje has found various problems for you to solve. As always, the winner is entitled to a homebaked cake made by our president, Guus Frijters.

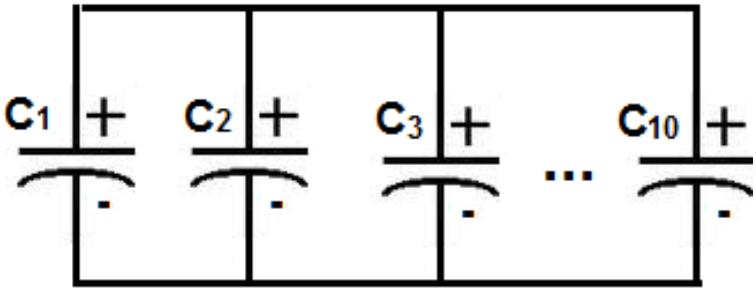


Part

The figure below can be cut into two parts with equal form and size. You may cut it however you want, as long as you end up with only two parts.

20 capacitors

On the table there are 20 capacitors, ten of which are placed with the + side to the right and ten have the - side to the right. However, the lights stopped working, and Truusje has no way to see or feel which capacitors are which. How can Truusje create two parallel circuits, where both circuits have an equal capacitance? She may divide the capacitors in any groups she wants, plug them into a breadboard in any way she wants.
A capacitor with reversed polarity won't add to the capacitance of the circuit.



Poison at the winetasting

24 hours before the winetasting event the board finds out that one of the 150 bottles was poisoned. After drinking even a little bit of the poisoned wine, death occurs within 10 to 20 hours. In order to save all the other members of Scintilla, how many members does the board need to sacrifice to test the wines before the winetasting event?

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AME is an independent developer and manufacturer of high quality electronic products located in the top technological region of the world (Brainport Eindhoven). Our goal is to create innovative products that exceed customer expectations. We accomplish this by integrating product development and manufacturing and keeping a clear focus on the product and its function. Driven by technology, we strive for the best solution combining the disciplines of electrical, mechanical, software and industrial engineering. Through creativity, passion, ambition, motivation and a highly educated level of our employees AME secures its goal of being a profitable company.

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AME is the ideal work environment to develop hands-on experience while completing your studies. You will be involved in challenging real-world projects and work with experts from a multitude of technological disciplines. We invite you to get in touch with us to discuss any internship openings.

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